

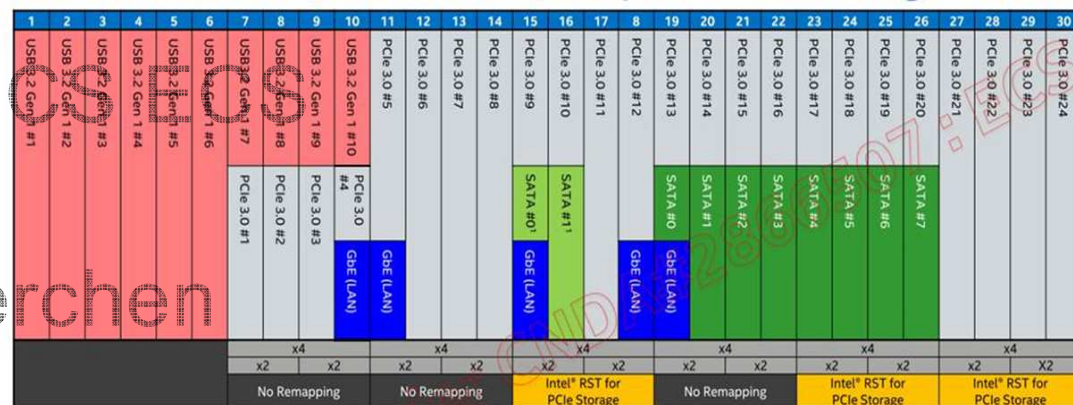


**ECS**  
**CONFIDENTIAL**

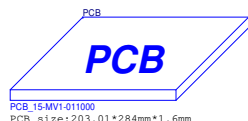
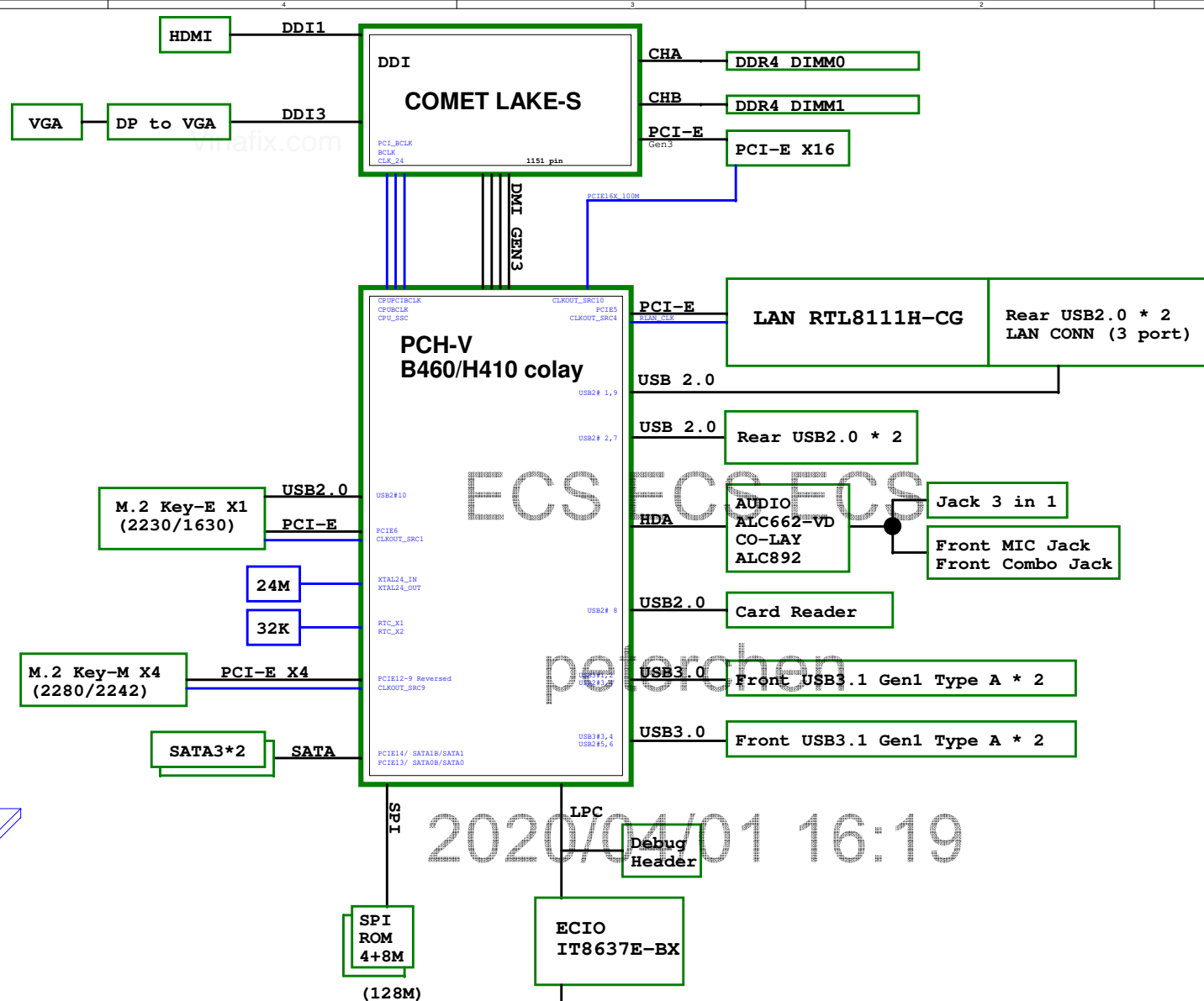
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[illegible]

Intel® RST for  
PCIe Storage po  
configurable as  
x2/x4 M.2



System Wake-up Capability Table

Power State	Commercial					
	S3	Deep Power Off Mode Disabled S4	S5	Deep Power Off Mode Enabled S4	S5 <sup>1</sup>	G3 to S5
Wake-up Event						
System Power Button	Yes	Yes	Yes	Yes	Yes	Yes
Monitor Power Button <sup>2</sup>	Yes	Yes	Yes	Yes	Yes	Yes
Onboard LAN Wake	Yes	Yes	Yes	Yes	Yes	Yes
PCIe Wake	Yes	Yes	Yes	Yes	No	No
PCI PME	Yes	Yes	Yes	Yes	No	No
RTC Alarm	Yes	Yes	Yes	Yes	No	No
PS/2 Keyboard/Mouse	Yes	Yes	Yes	Yes	No	No
USB Keyboard/Mouse	Yes	Yes	No	Yes	No	No
Modem Ring	Yes	Yes	Yes	Yes	No	No

Power State	Consumer					
	S3	Deep Power Off Mode Disabled S4	S5	Deep Power Off Mode Enabled S4	S5 <sup>1</sup>	G3 to S5
Wake-up Event						
System Power Button	Yes	Yes	Yes	Yes	Yes	Yes
Monitor Power Button <sup>2</sup>	No	No	No	No	No	No
Onboard LAN Wake	Yes	Yes	Yes	Yes	No	No
PCIe Wake	Yes	Yes	Yes	Yes	No	No
PCI PME	No	No	No	No	No	No
RTC Alarm	Yes	Yes	Yes	Yes	No	No
PS/2 Keyboard/Mouse	No	No	No	No	No	No
USB Keyboard/Mouse	Yes	No	No	No	No	No
Modem Ring	No	No	No	No	No	No

## PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPP_A0	+3P3V_SB	KBRST_L_RC	RCIN#
GPP_A1	+3P3V_SB	LPC_LAD0	LAD0
GPP_A2	+3P3V_SB	LPC_LAD1	LAD1
GPP_A3	+3P3V_SB	LPC_LAD2	LAD2
GPP_A4	+3P3V_SB	LPC_LAD3	LAD3
GPP_A5	+3P3V_SB	LPC_FRAME_L	LFRAME#
GPP_A6	+3P3V_SB	SERIRQ	PIRQA#
GPP_A7	+3P3V_SB	PIRQA_L	PIRQA#
GPP_A8	+3P3V_SB	CLKRUN#	CLKRUN#
GPP_A9	+3P3V_SB	PCH_SIO_24M	CLKOUT_LPC 0
GPP_A10	+3P3V_SB	PCH_LPC_24M	CLKOUT_LPC 1
GPP_A11	+3P3V_SB	PME_L	PME#
GPP_A13	+3P3V_SB	SUSWARN	SUSWARN#
GPP_A15	+3P3V_SB	SUSACK_L	SUSACK#
GPP_B3	+3P3V_SB	BT_DISABLE_L	GP-In
GPP_B6	+3P3V_SB	M2CLK_REOT_L	GP-In
GPP_B8	+3P3V_SB	H_SKTOCC_L	GP-In
GPP_B9	+3P3V_SB	RLAN_CLKREQ#	GP-In
GPP_B11	+3P3V_SB	EXT_C10_GATE_N (for CEC)	GP-Out
GPP_B12	+3P3V_SB	SLP_S0_L	SLP_S0#
GPP_B13	+3P3V_SB	PCH_PLTRST_L	PLTRST#
GPP_B14	+3P3V_SB	PCH_SPKR	SPKR
GPP_C0	+3P3V_SB	SMBCLK_STBY	SMBCLK
GPP_C1	+3P3V_SB	SMBDATA_STBY	SMBDATA
GPP_C3	+3P3V_SB	SML0_CLK	SML0CLK
GPP_C4	+3P3V_SB	SML0_DATA	SML0DATA
GPP_C6	+3P3V_SB	SML1_CLK	SML1CLK
GPP_C7	+3P3V_SB	SML1_DATA	SML1DATA
GPP_D4	+3P3V_SB	PC_HEALTH	GP-In
GPP_D6	+3P3V_SB	GPP_D6_BIOSWP	GP-In
GPP_D7	+3P3V_SB	GPP_D7_CASEOPEN	GP-In
GPP_E0	+3P3V_SB	OBR_L	GP-In
GPP_E7	+3P3V_SB	GPP_E7_THERM	GP-In
GPP_E8	+3P3V_SB	SATALED_L	GP-In
GPP_F7	+3P3V_SB	DGPU_SEL_N (for CEC)	GP-In
GPP_F8	+3P3V_SB	DGPU_PWR_EN_R_N (for CEC)	GP-In
GPP_F9	+3P3V_SB	DGPU_PWR_OK_R (for CEC)	GP-In
GPP_F16	+3P3V_SB	GPP_F16 (USB power enable)	GP-In
GPP_F22	+3P3V_SB	GPP_F22_PCIEIRST (for CEC)	GP-In
GPP_F23	+3P3V_SB	GPP_F23_PCIEIRST (for CEC)	GP-In
GPP_G1	+3P3V_SB	PCH_RL_L	GP-In
GPP_G10	+3P3V_SB	PCH_RST_GPIO_C10 (for CEC)	GP-In
GPP_G16	+3P3V_SB	LPC_PME_L	GP-In
GPP_G22	+3P3V_SB	GPP_G22_PCIEI16_CEC (for CEC)	GP-In
GPP_H3	+3P3V_SB	M2_2280_CLKREQ09_L	GP-In
GPP_H4	+3P3V_SB	PCIE16X_CLKREQ_L_R	GP-In
GPP_H7	+3P3V_SB	GPP_H7_PCIEIRST (for CEC)	GP-In
GPP_H8	+3P3V_SB	GPP_H8_PCIEIRST (for CEC)	GP-In
GPP_H13	+3P3V_SB	GPP_H13 (BOM Detect)	GP-In
GPP_H14	+3P3V_SB	GPP_H14 (Acer GPIO Reserve)	GP-In
GPP_H15	+3P3V_SB	GPP_H15 (Acer GPIO Reserve)	GP-In
GPP_H17	+3P3V_SB	GPP_H17 (BOM Detect)	GP-In
GPP_H18	+3P3V_SB	GPP_H18 (BOM Detect)	GP-In
GPP_H23	+3P3V_SB	PCH_PS_ON_B	PS_ON#
GPP_I0	+3P3V_SB	DDPB_HPD0	GP-In
GPP_I2	+3P3V_SB	DDPD_HPD	GP-In
GPP_I4	+3P3V_SB	GPO_L	GP-In
GPP_I5	+3P3V_SB	DDIB_CTRLCLK	GP-In
GPP_I6	+3P3V_SB	DDIB_CTRLDATA	GP-In
GPP_I9	+3P3V_SB	WLAN_DISABLE_L	GP-In
GPP_I10	+3P3V_SB	GPP_I10_S0IX_SSD (for CEC)	GP-Out
GPD0	+3P3V_DSW	RLAN_PWR_EN	BATLOW#
GPD3	+3P3V_DSW	PCH_PWRON_L	PWRBNT#
GPD4	+3P3V_DSW	SLP_S3_L	SLP_S3#
GPD5	+3P3V_DSW	SLP_S4_L	SLP_S4#
GPD6	+3P3V_DSW	SLP_AMT_L	SLP_A#
GPD8	+3P3V_DSW	SUSCLK	SUSCLK
GPD9	+3P3V_DSW	GPD9 (ME disable)	SLP_WLAN#
GPD10	+3P3V_DSW	SLP_S5_L	SLP_S5#

update 1022

## ECIO-GPIO function

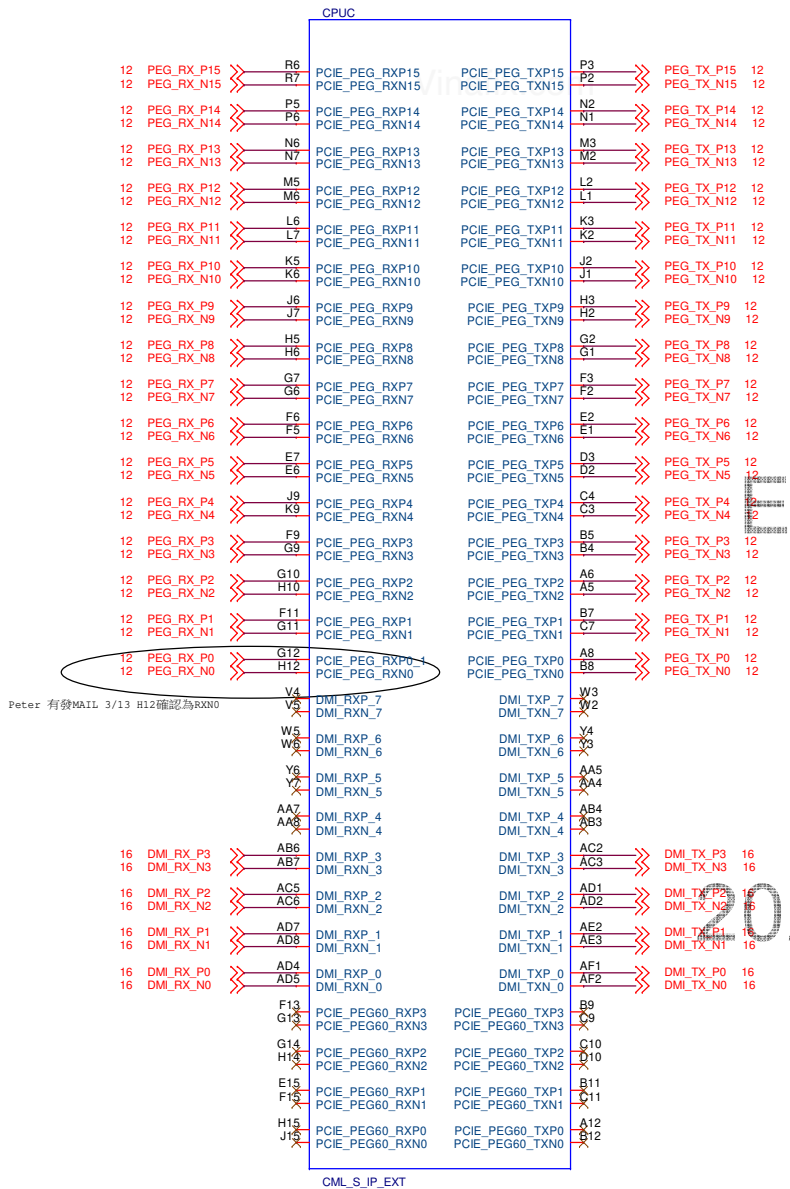
Pin Name	Power Well	Usage	Default Status
GP16	+3P3V_SB	basic health function	5VSB_CTRL#
GP17	+5V_DSW	VGA Wake Control by BIOS	RI2#
GP35	+3P3V_DSW	ACER Power ON by Monitor (HDMI)	F_DIO3
GP36	+3P3V_DSW	ACER Power ON by Monitor (VGA)	FAN_CTL3
GP41	+3P3V_DSW	EC_RTCRST	PWROK2
GP46	+3P3V_SB	Thermal Shutdown	SMCLK2
GPA6	+5V_DSW	HDMI Wake Control by BIOS	GPIO

## PCH\_CPU-Strap

Pin Name	Usage	Default Status
CFG0	CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted	1 = (Default) Normal Operation
CFG1	CFG[1]: Reserved configuration lane	
CFG2:5:6	CFG[2]:1 = Normal operation CFG[6:5]:11 = 1 x16 PCI Express	Normal operation PCIE16X
CFG3	CFG[3]: Reserved configuration lane.	
CFG4	CFG[4]: eDP disable :	eDP Enable
CFG7	CFG[7]: PEG Training	1 = (default) PEG Train immediately following RESET# de-assertion.
CFG19:8	CFG[19:8]:Reserved configuration lanes.	
SPKR/GPP_B14	Top Swap Override	0 =Disable "Top Swap" mode. (Default)
GSPI0_MOSIGPP_B18	No Reboot	0 =Disable "No Reboot" mode
SMBALERT#/GPP_C2	Flash Descriptor Security Override	0 =Disable Flash Descriptor Security (overide). 1 =Enable security measures defined in the Flash Descriptor. (Default)
GSPI1_MOSIGPP_B22	Boot BIOS Strap Bit BBS	0=SPI
SML0ALERT#/GPP_C5	eSPI or LPC	0 =LPCis selected for SIO.
HDA_SDO	Flash Descriptor Security Override	This signal has a weak internal pull-down. 0 =Enable security measures defined in the Flash Descriptor. (Default) 1 =Disable Flash Descriptor Security (overide). This strap should only be asserted high using external pull-up in manufacturing/debug environments only.
SPI0_MISO	Reserved	0 = JTAG GDT 1 = Normal (Default) V
GPP_B23/SML1ALERT#/PCHHOT#	Intel® DCI-1	1 = Enable DCI. (CWB/Datasheet)
GPP_H12/SML2ALERT#	Reserved	0 = Attached Flash Sharing (HAPS) enable (Default)
SPI0_MOSI	Reserved	0 = Boot Salt 1 = Normal (Default)
SPI0_IO2	Reserved	1 = Consent strap disable (Default)
SPI0_IO3	Reserved	1 = Personality strap disable (Default)

## Interrupt mapping

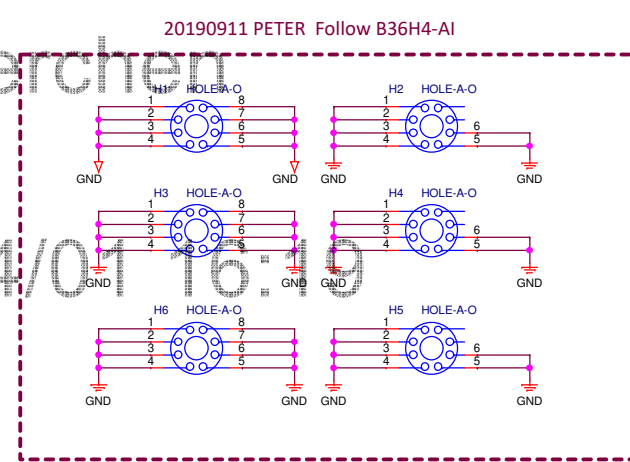
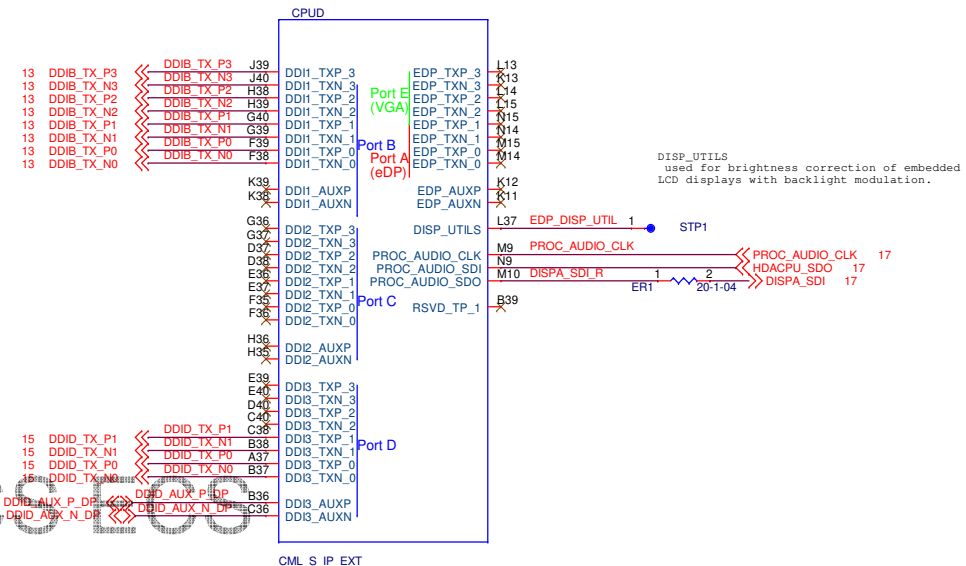
Function	INT#port	PCIe#1 port	Device
M.2 SSD (Q-bay)		PCIe 5,6,7,8 (H410)	M2_2
M.2 SSD		PCIe 21,22,23,24 (B460)	M2_3
LAN		PCIe 11	RTL8111H-CGS
M.2 WIFI		PCIe 12	M2_1
SATA		PCIe 13 (SATA1)	SATA1
SATA		PCIe 14 (SATA2)	SATA2



HDMI

DP1

DP to VGA







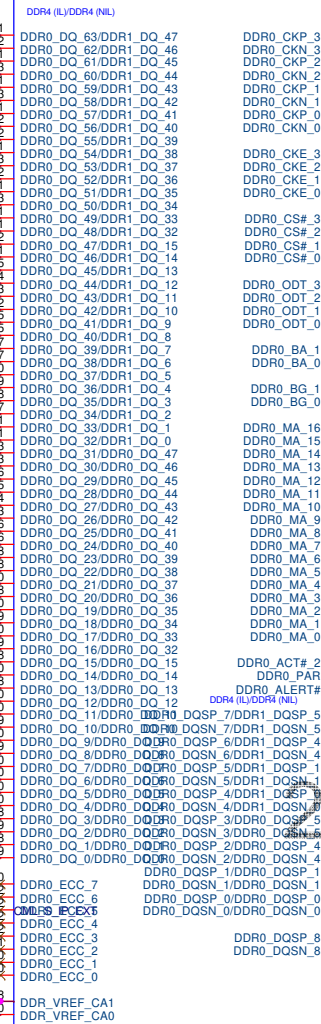
# DDR4 CH.A

9 M\_DATA\_A[0..63] << M\_DATA\_A[0..63]  
 9 M\_CLK\_A\_P[0..1] << M\_CLK\_A\_P[0..1]  
 9 M\_CLK\_A\_N[0..1] << M\_CLK\_A\_N[0..1]  
 9 M\_CKE\_A[0..1] << M\_CKE\_A[0..1]  
 9 M\_CS\_A\_L[0..1] << M\_CS\_A\_L[0..1]  
 9 M\_ODT\_A[0..1] << M\_ODT\_A[0..1]  
 9 M\_MA\_A[0..16] << M\_MA\_A[0..16]  
 9 M\_DQS\_A\_P[0..7] << M\_DQS\_A\_P[0..7]  
 9 M\_DQS\_A\_N[0..7] << M\_DQS\_A\_N[0..7]

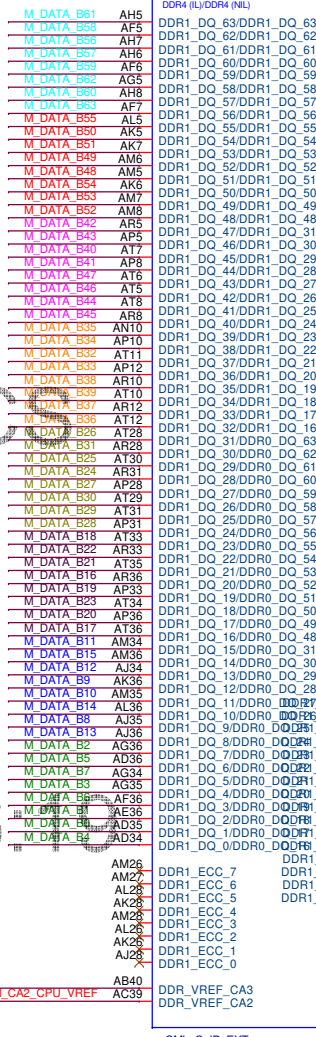
# DDR4 CH.B

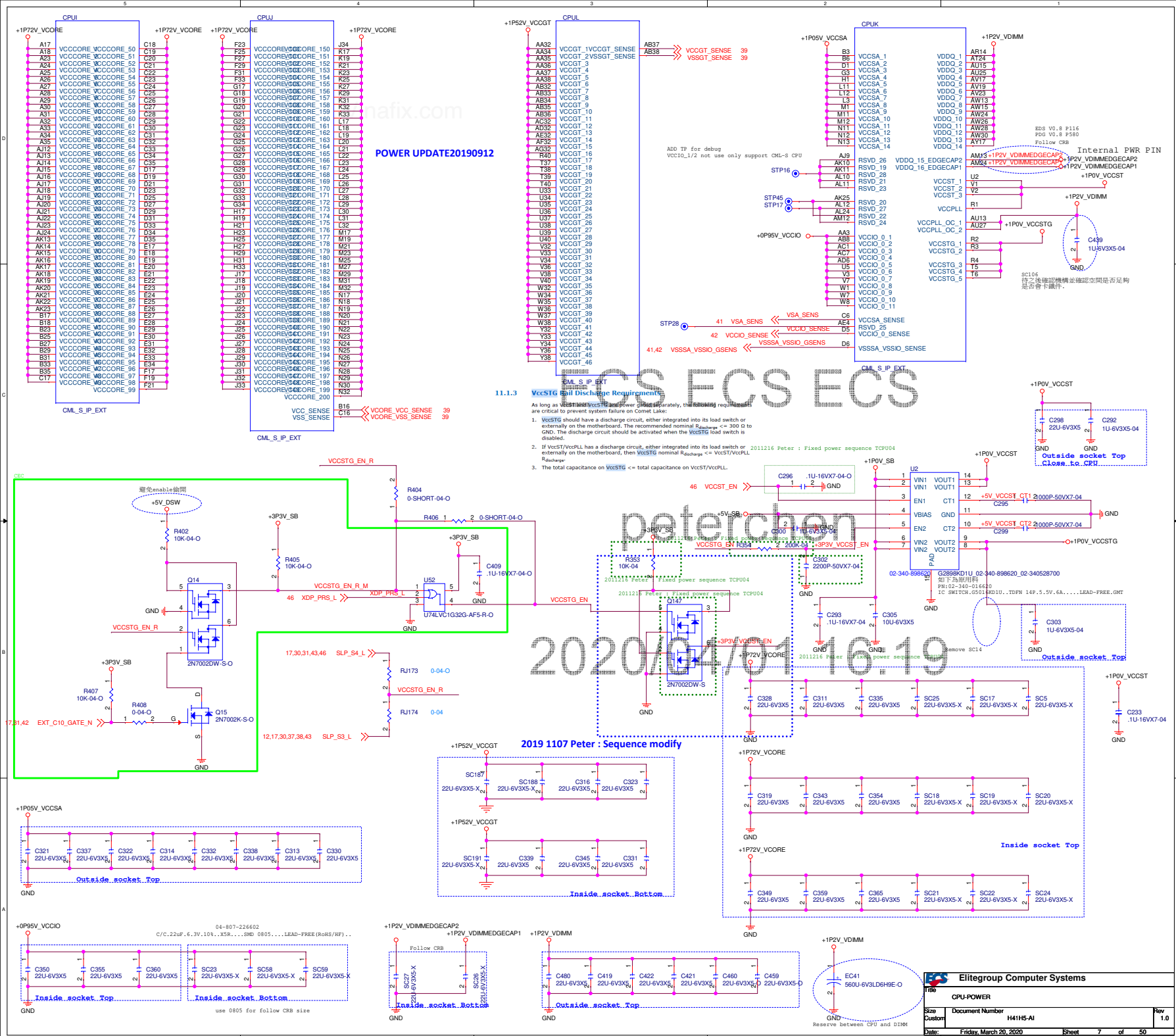
10 M\_DATA\_B[0..63] << M\_DATA\_B[0..63]  
 10 M\_CLK\_B\_P[0..1] << M\_CLK\_B\_P[0..1]  
 10 M\_CLK\_B\_N[0..1] << M\_CLK\_B\_N[0..1]  
 10 M\_CKE\_B[0..1] << M\_CKE\_B[0..1]  
 10 M\_CS\_B\_L[0..1] << M\_CS\_B\_L[0..1]  
 10 M\_ODT\_B[0..1] << M\_ODT\_B[0..1]  
 10 M\_MA\_B[0..16] << M\_MA\_B[0..16]  
 10 M\_DQS\_B\_P[0..7] << M\_DQS\_B\_P[0..7]  
 10 M\_DQS\_B\_N[0..7] << M\_DQS\_B\_N[0..7]

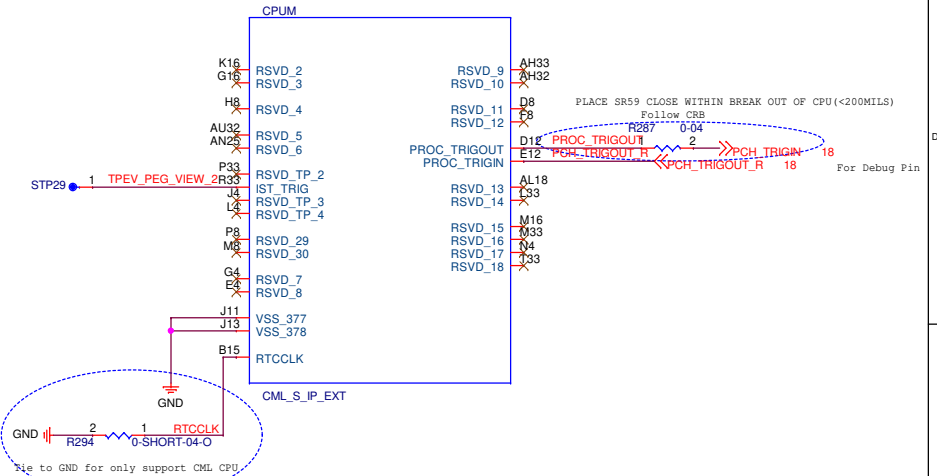
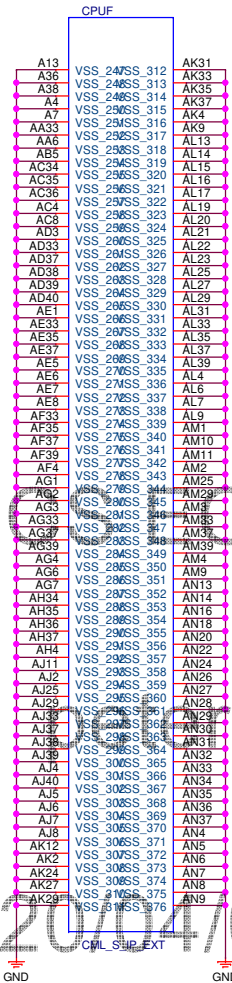
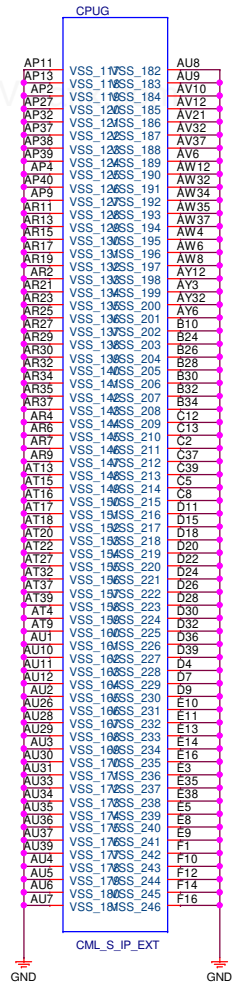
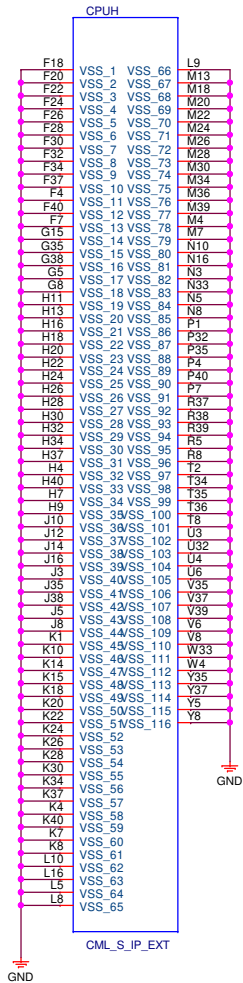
CPUA



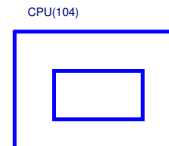
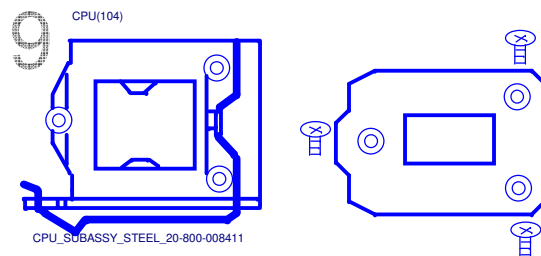
CPUB







Del U54,FB24,FB25 for only support CML CPU



check  
???尚未確認料  
Symbol 待修改???

CPU\_Rerention-O

1200	Lotes	SUBASSY.STEEL...LGA 12XX..W/BACK PLATE,NI.....AZIF0208-P001C...HF.LEAD-FREE.LOTES	0.67
		20-800-008411	
1200	Foxconn	SUBASSY.STEEL...LGA 12XX..W/BACK PLATE.....WNN6A61-11NK0-4H...HF.LEAD-FREE.FOXCONN	0.7
		20-800-008511	

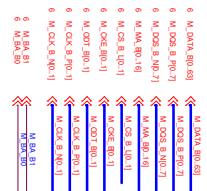
Elitegroup Computer Systems			
Title CPU-GND			
Size	Document Number	Rev	
Custom	H41H5-AI	1.0	
Date:	Friday, March 20, 2020	Sheet	8 of 50







DDIM4 CH1\_B



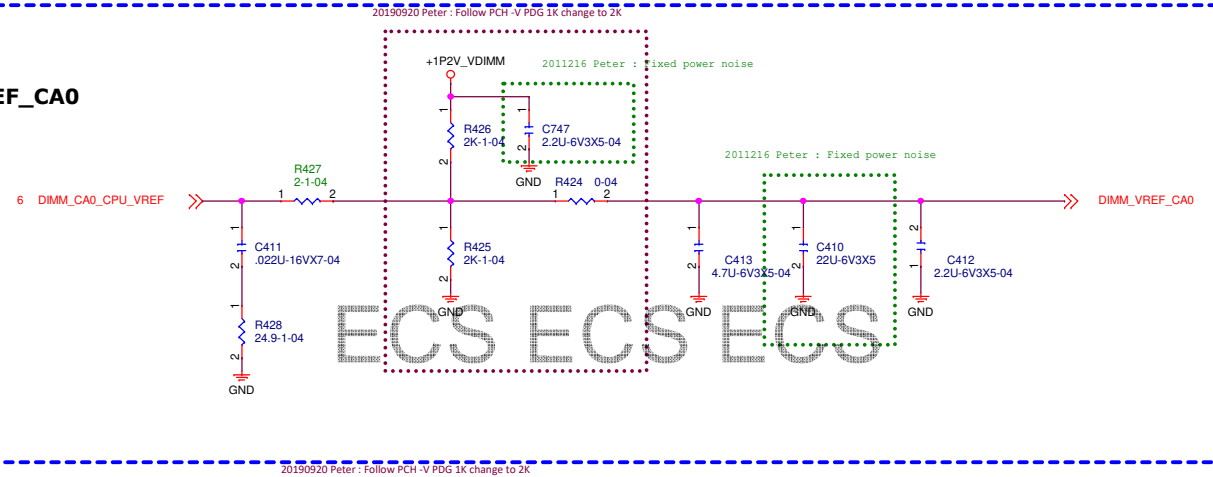
# NOTE

CA[0] 接給CHA-DIMM0/1  
CA[2] 接給CHB-DIMM0/1  
CA[1][3] 不上件For not sup next gen CPU

Vinafix.com

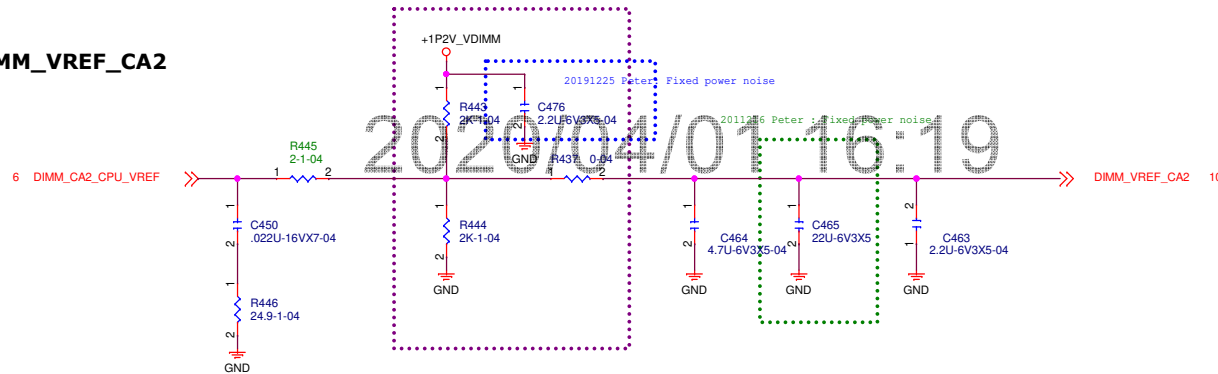
## CHA

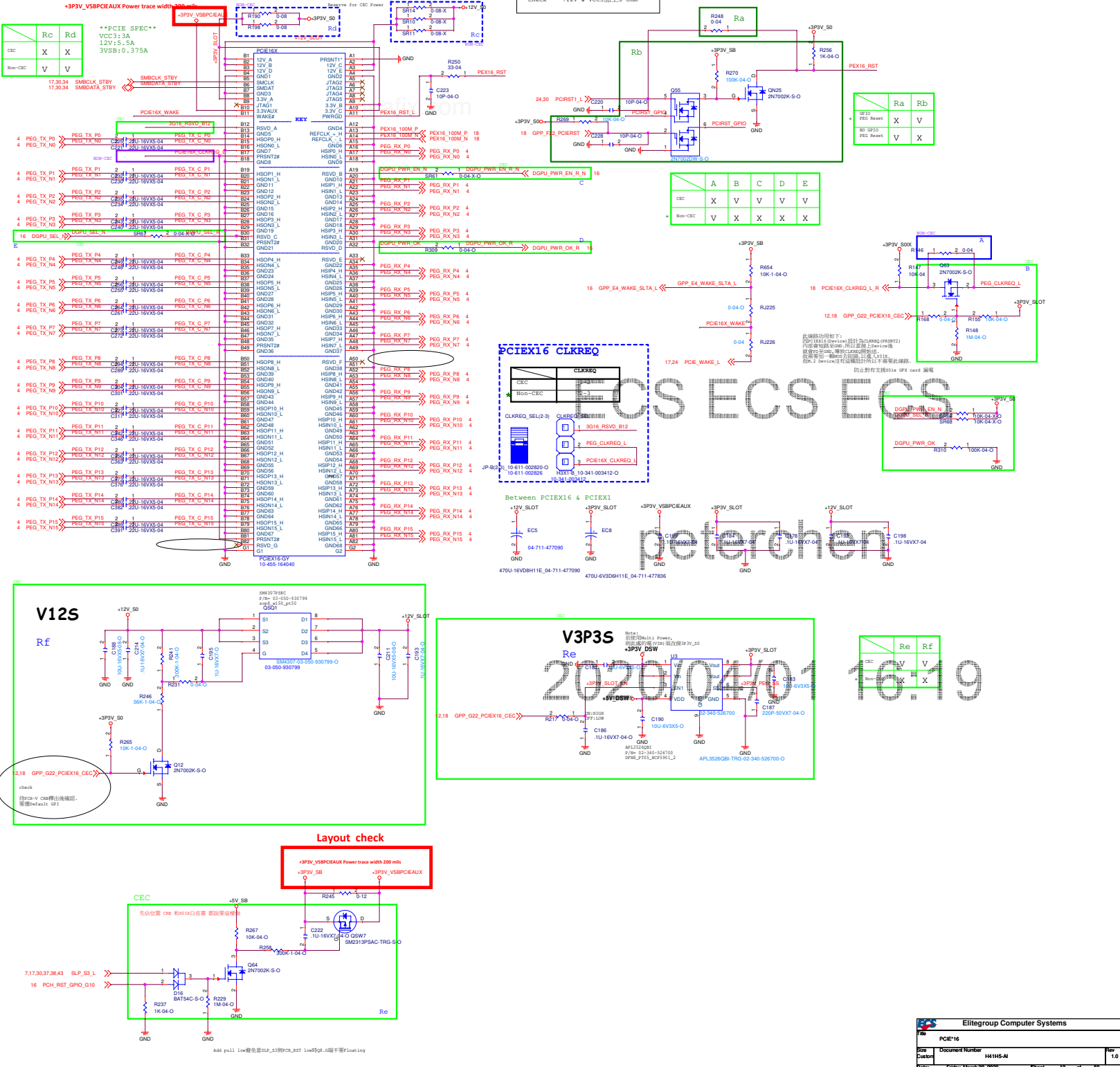
### DIMM\_VREF\_CA0



## CHB

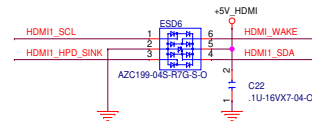
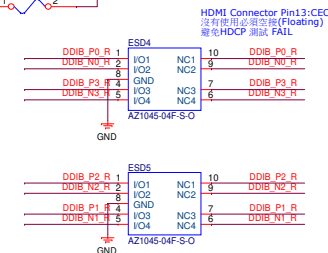
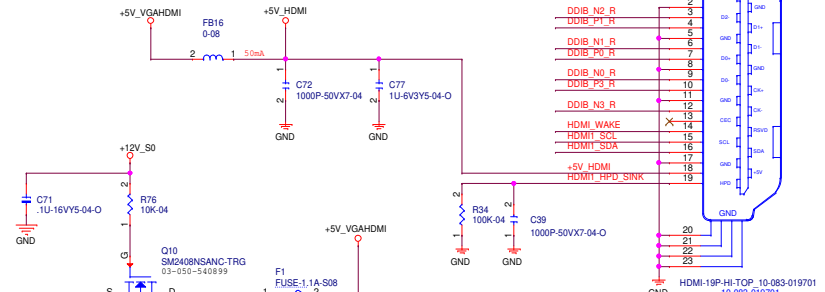
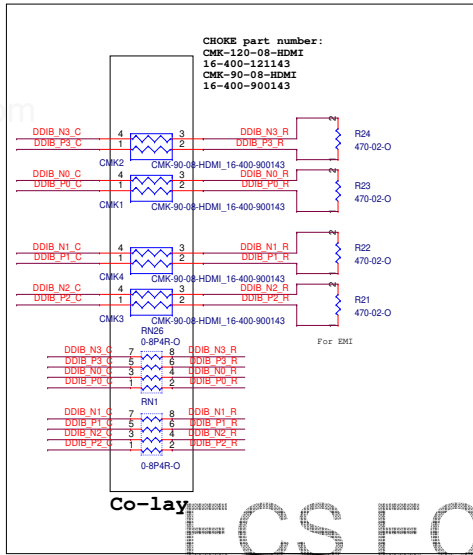
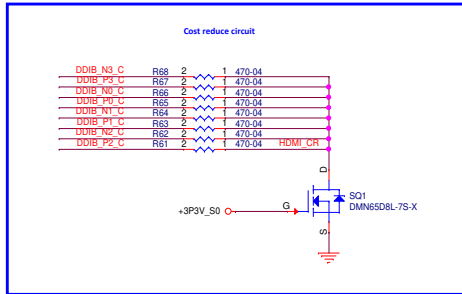
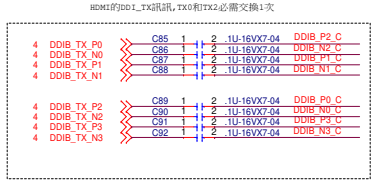
### DIMM\_VREF\_CA2



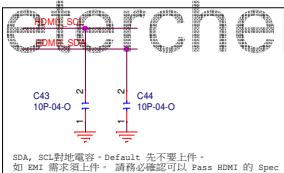
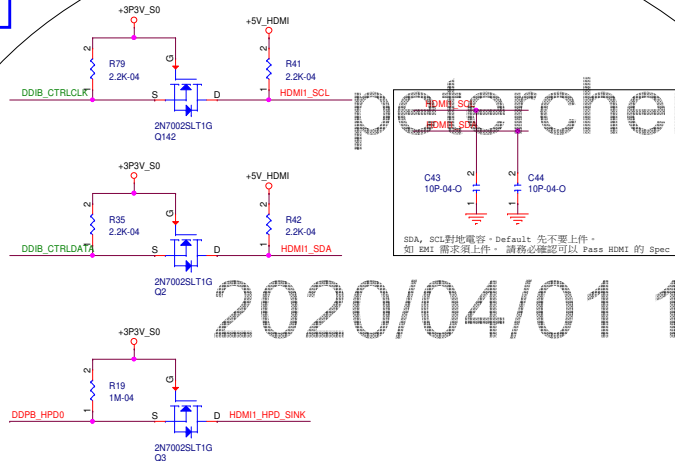


# HDMI 1

2010906 Peter: 因HDMI resolution suport 1920x1080 only  
Removed ASM1442K circuit , Add cost reduce circuit



When ESD link to "wake up by monitor" signal, please select AZC199  
Reason:  
In system S3-S5, ESD no power supply, so "wake up by monitor" signal keep to Low.  
System caused not wake up.



2020/04/01 16:19

for matching technology, refer to General Electrical Design Guidelines on page 30.

5.1.9 Digital Display Interface Disabling and Termination Guidelines

All the digital display ports on the Comet Lake processor have a strap associated with it. The port strap needs to be set to configure each digital port irrespective of the digital display technology HDMI/DP. The following table lists all the digital display straps and guidelines to enable/disable a respective port on the platform. All the straps are sampled on the rising edge of the PWROK signal.

Table 38. DDI Disabling and Termination Guidelines

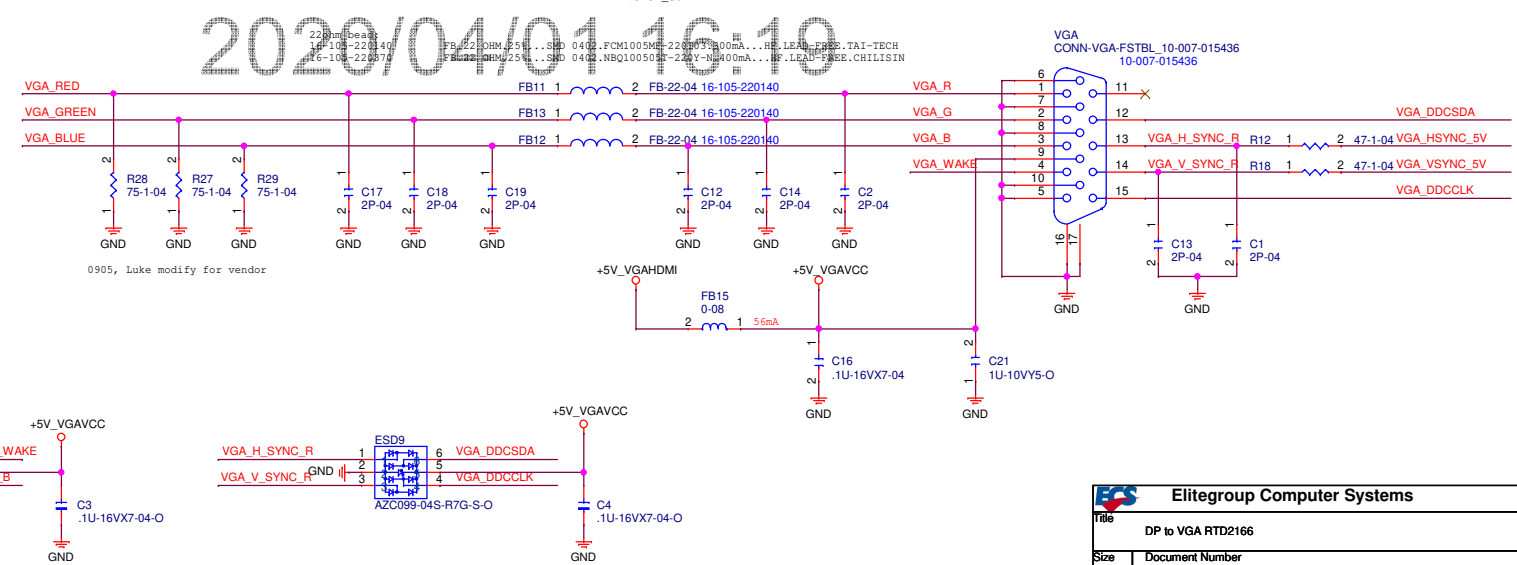
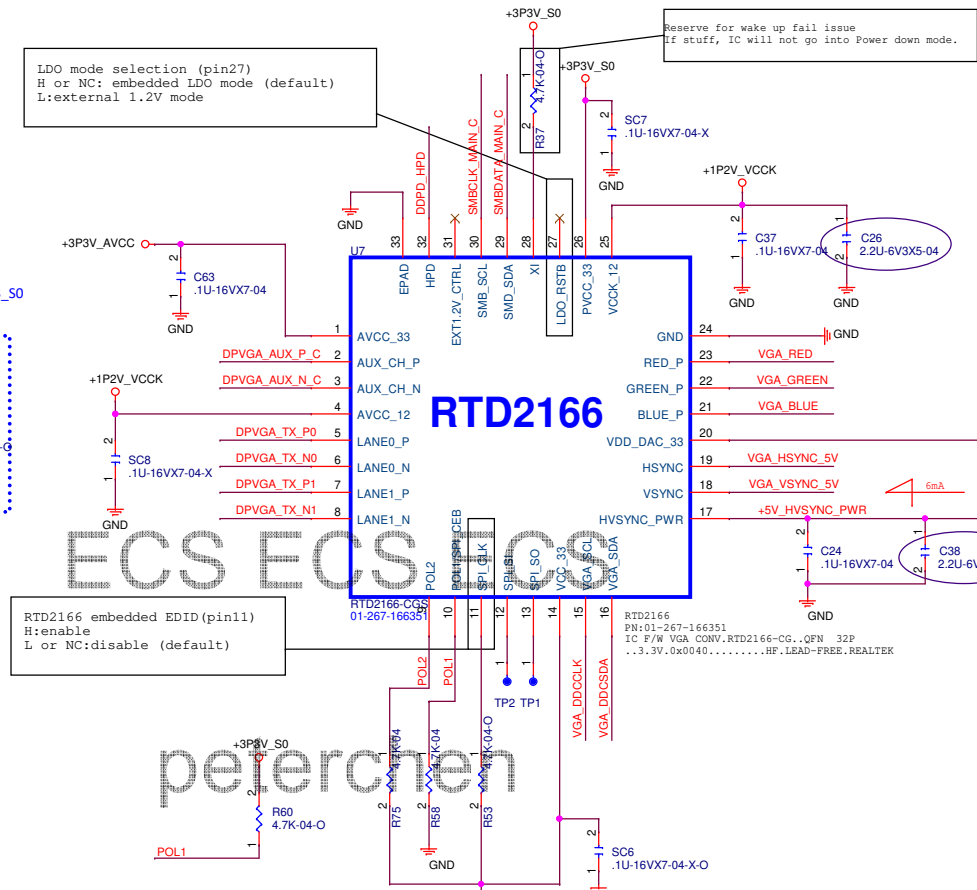
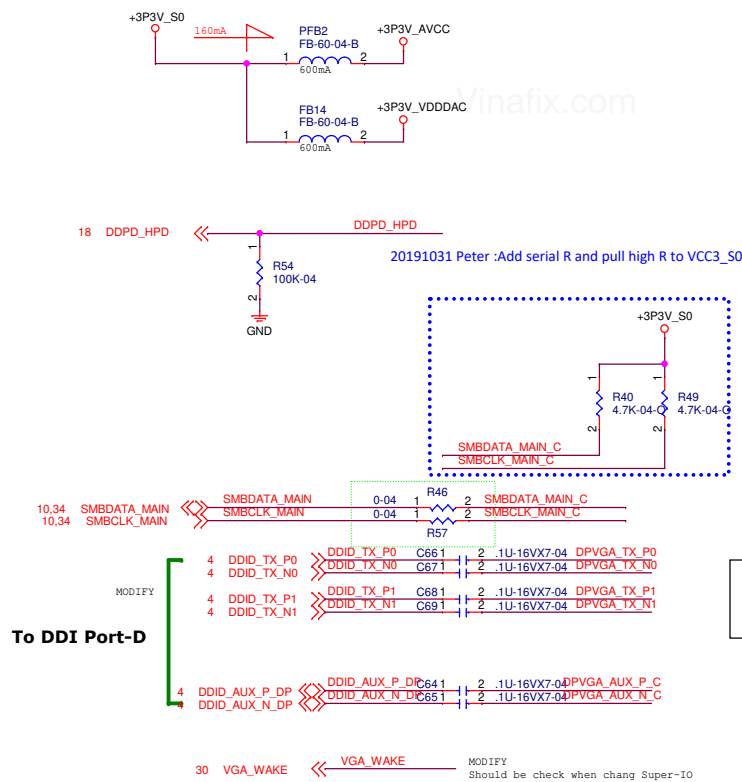
Port	Strap	How to Enable Port	How to Disable Port
Port 1	DDPB_CTRLDATA	Pull up to 3.3V with 2.2K ohm $\pm 5\%$ resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3V with 2.2K ohm $\pm 5\%$ resistor	No Connect
Port 3	DDPD_CTRLDATA	Pull up to 3.3V with 2.2K ohm $\pm 5\%$ resistor	No Connect

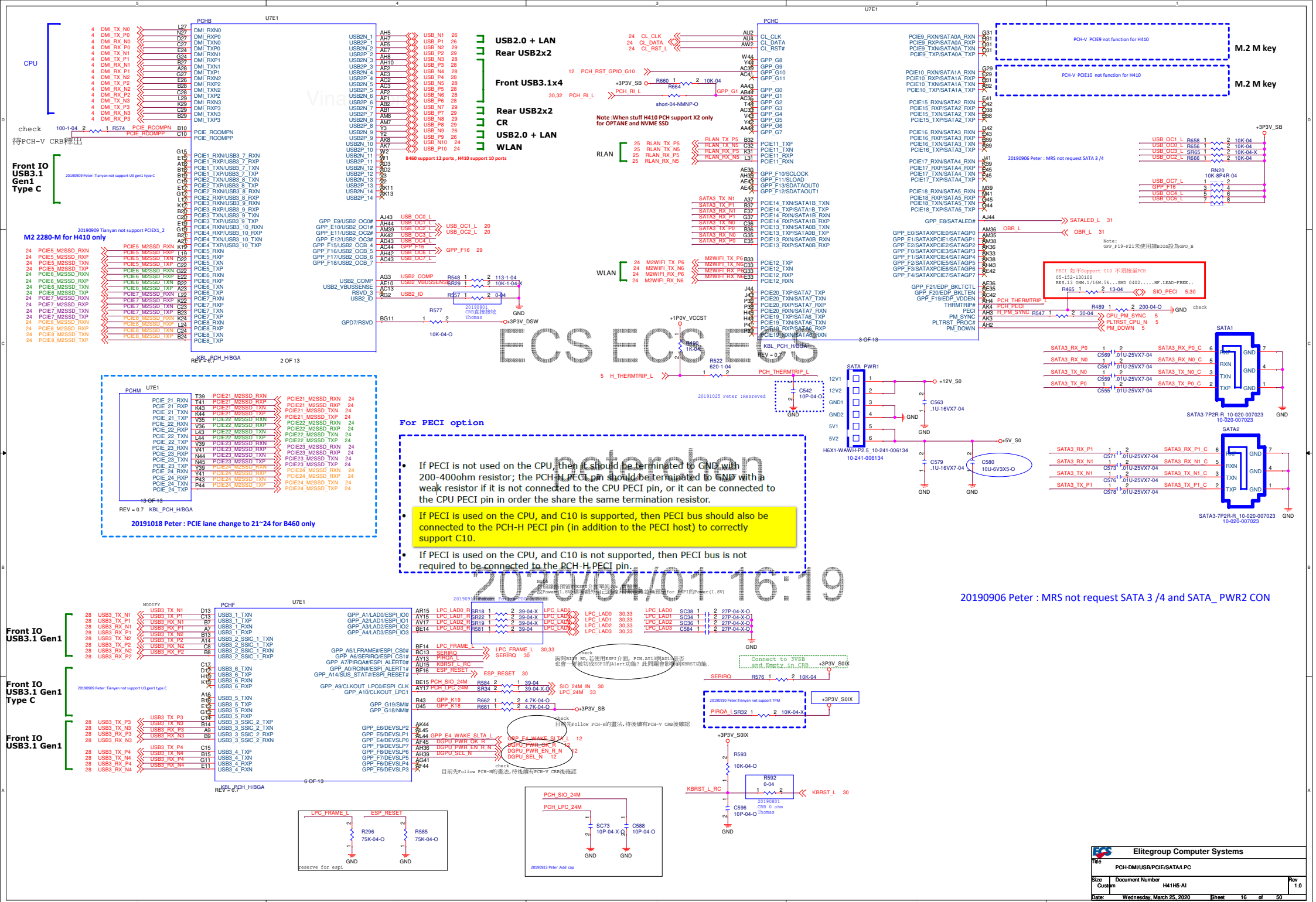
The following table lists connection details for the digital display signals when Comet Lake processor graphics is disabled. When Comet Lake processor graphics is not implemented on the platform, the digital display interface must also be disabled in BIOS. Refer to the BIOS specification on how to disable the respective display interfaces.

Table 39. DDI Disabling and Termination Connections

Pin Name	Recommendation
DDPB_AUXP / DDPC_AUXP / DDPD_AUXP	No Connect
DDPB_AUXN / DDPC_AUXN / DDPD_AUXN	No Connect
DDPB_HPD / DDPC_HPD / DDPD_HPD	No Connect
DDI1_TXP[3:0] / DDI2_TXP[3:0] / DDI3_TXP[3:0]	No Connect
DDI1_TXN[3:0] / DDI2_TXN[3:0] / DDI3_TXN[3:0]	No Connect
DDPB_CTRLCLK / DDPB_CTRLDATA	No Connect
DDPC_CTRLCLK / DDPC_CTRLDATA	No Connect
DDPD_CTRLCLK / DDPD_CTRLDATA	No Connect

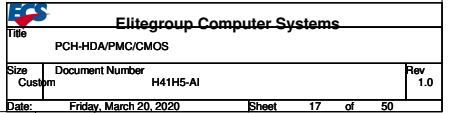


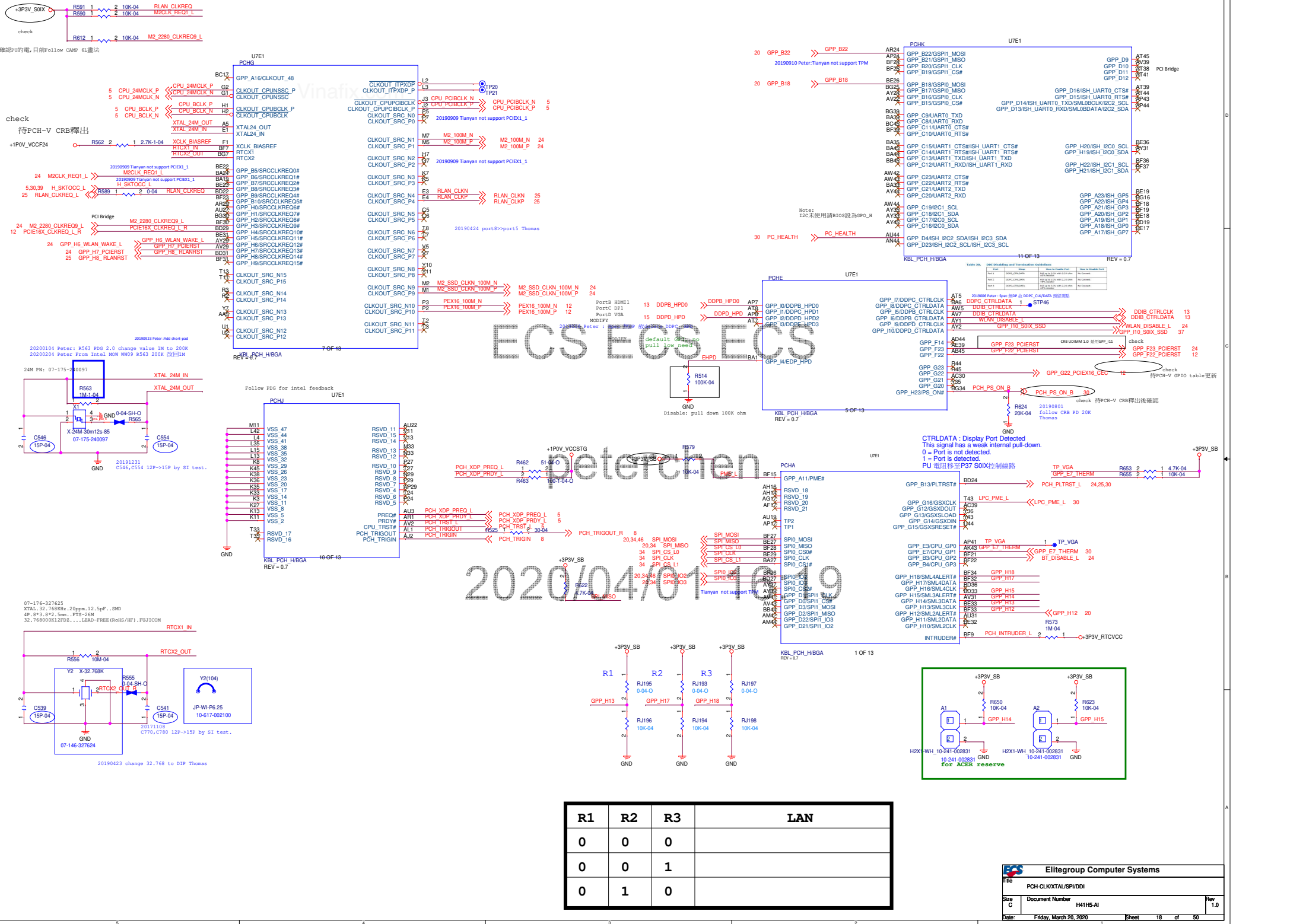




For PECI option

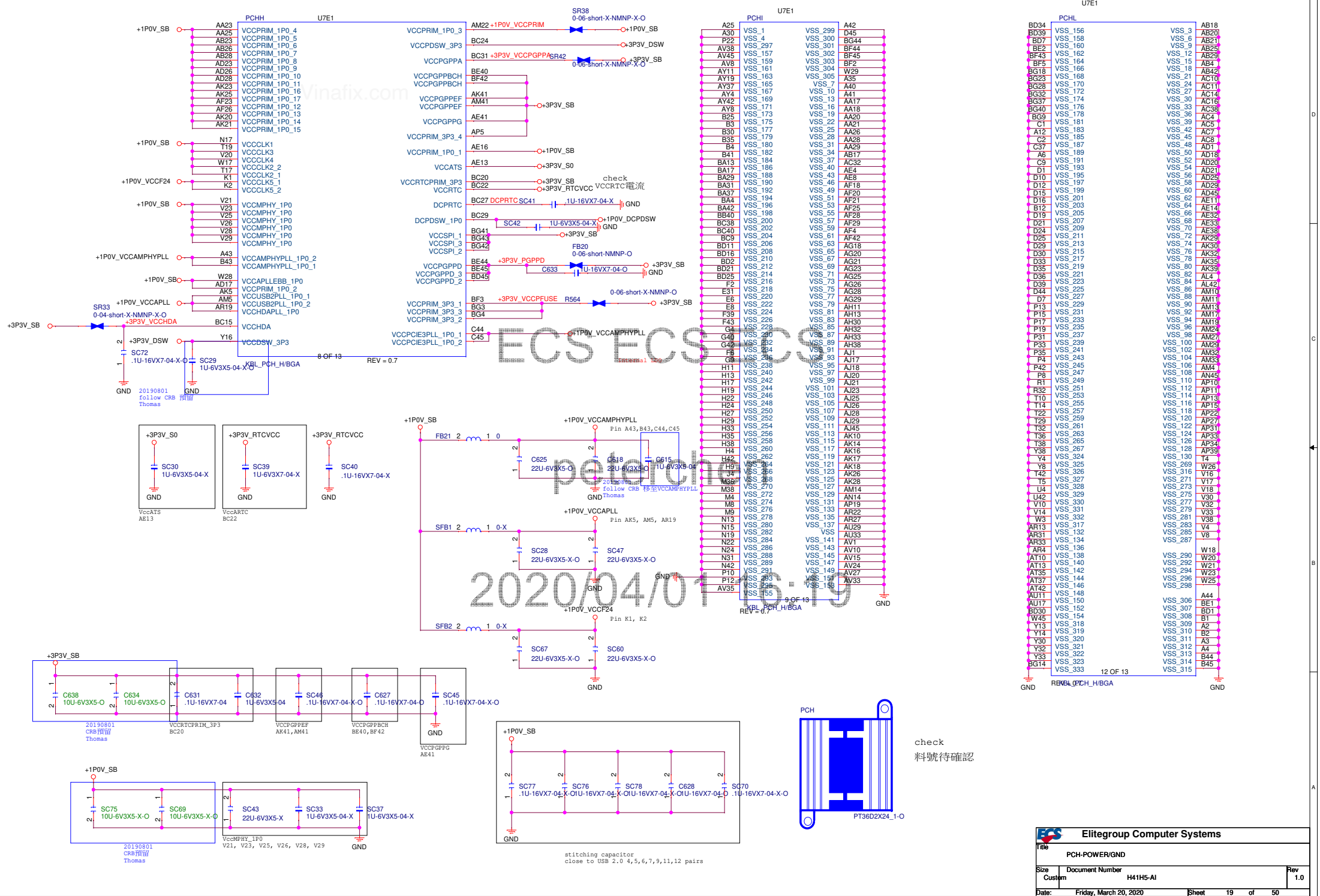
- If PECI is not used on the CPU, then it should be terminated to GND with 200-400ohm resistor; the PCH-H PECI pin should be terminated to GND with a weak resistor if it is not connected to the CPU PECI pin, or it can be connected to the CPU PECI pin in order to share the same termination resistor.
- If PECI is used on the CPU, and C10 is supported, then PECI bus should also be connected to the PCH-H PECI pin (in addition to the PECI host) to correctly support C10.
- If PECI is used on the CPU, and C10 is not supported, then PECI bus is not required to be connected to the PCH-H PECI pin.





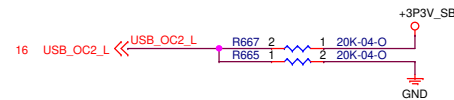
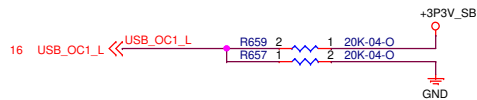
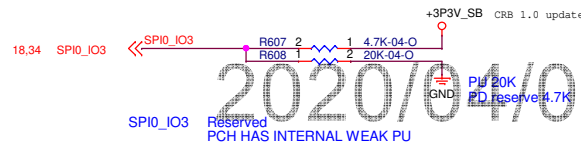
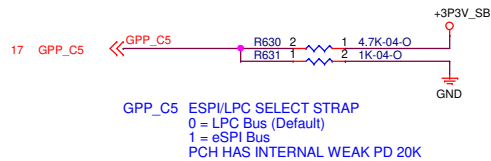
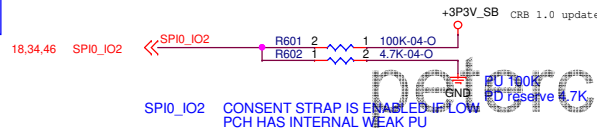
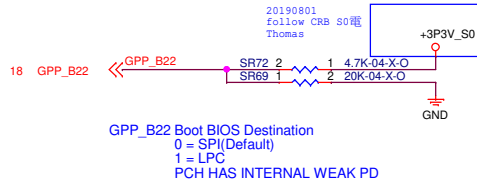
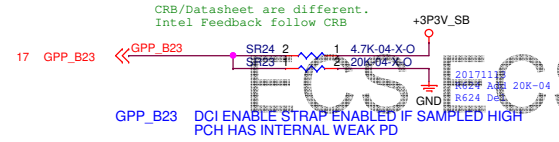
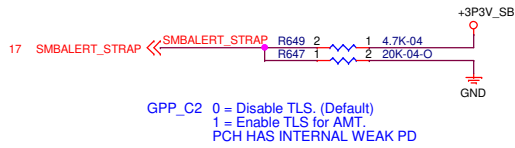
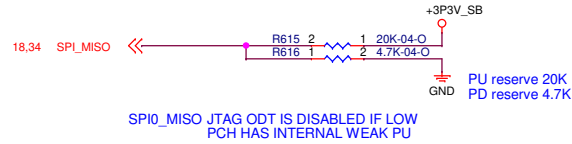
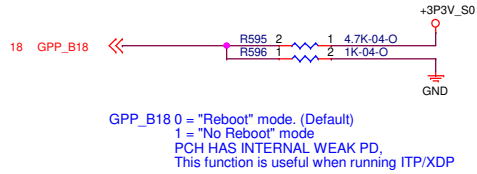
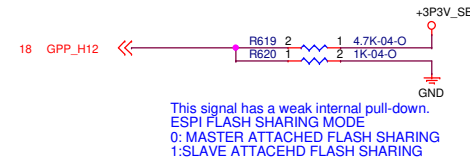
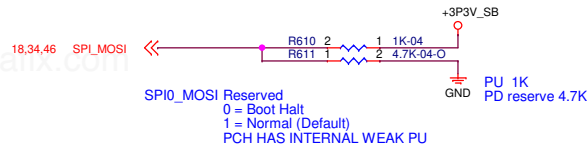
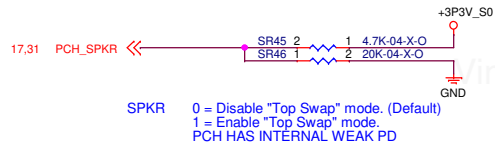
R1	R2	R3	LAN
0	0	0	
0	0	1	
0	1	0	





Elitegroup Computer Systems			
PCH-POWER/GND			
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20190801  
CRB 預留  
Thomas

PCIEX1\_1 PCIEX1\_2

Vinafix.com

20190909 Tianyan not support PCIEX1\_1, PCIEX1\_2

ECS ECS ECS

peterchen


2020/04/01 16:19

Vinafix.com

ECS ECS ECS

peterchen

2020/04/01 16:19

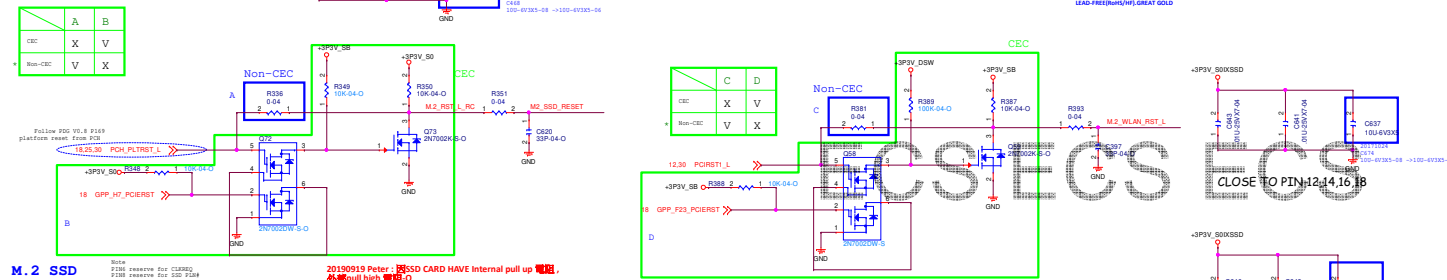
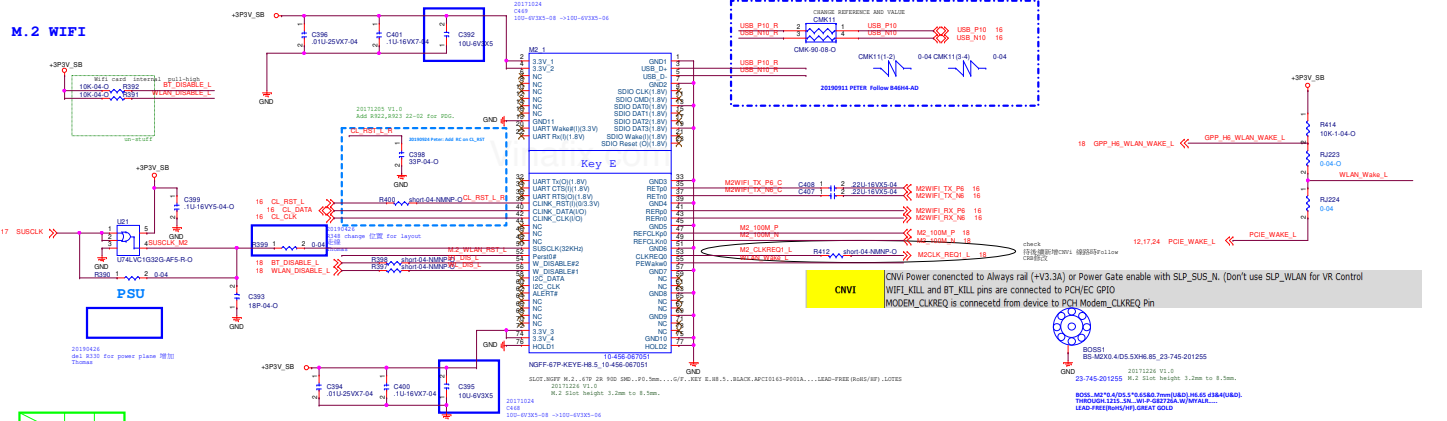
 Elitegroup Computer Systems			
Reserve(PCI Bridge)			
Size	Document Number	Rev	
Custom	H41H5-A1	1.0	
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ECS ECS ECS

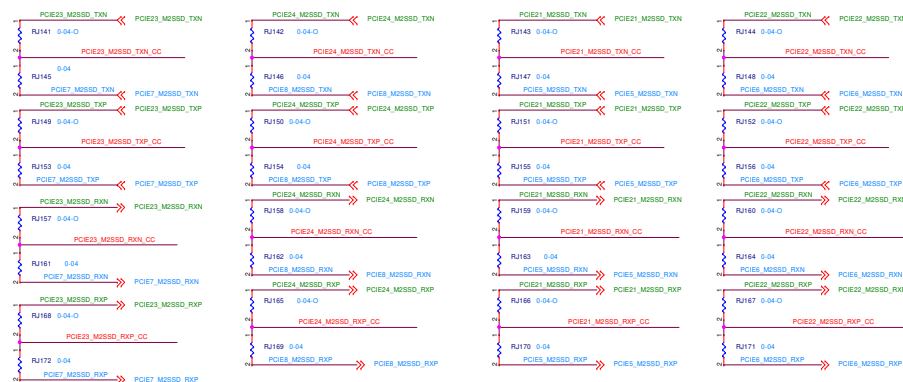
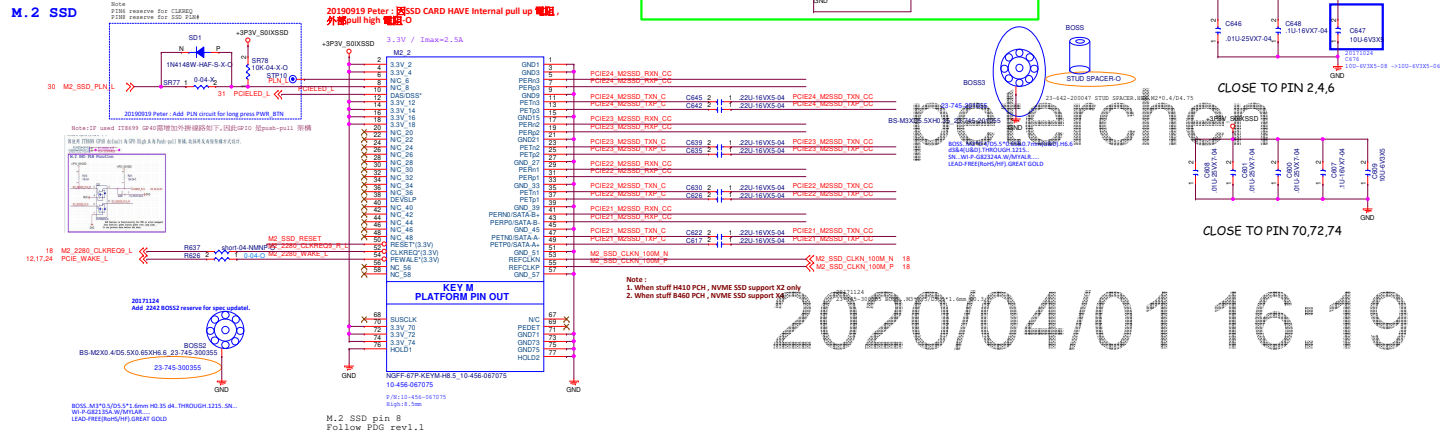
peterchen

2020/04/01 16:19

## M.2 WIFI



## M.2 SSD



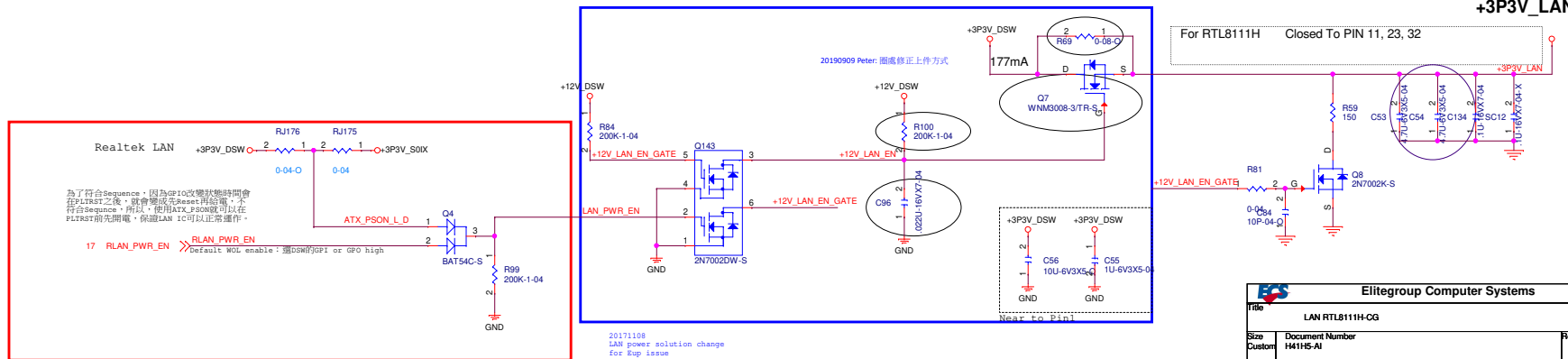
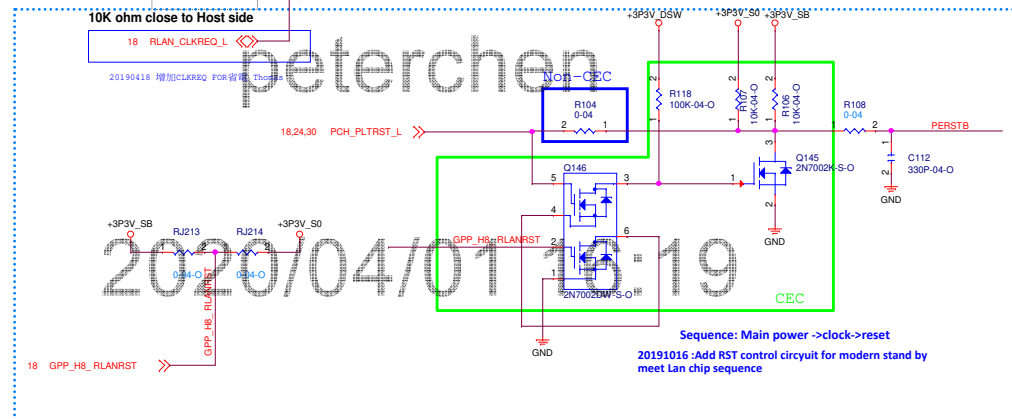
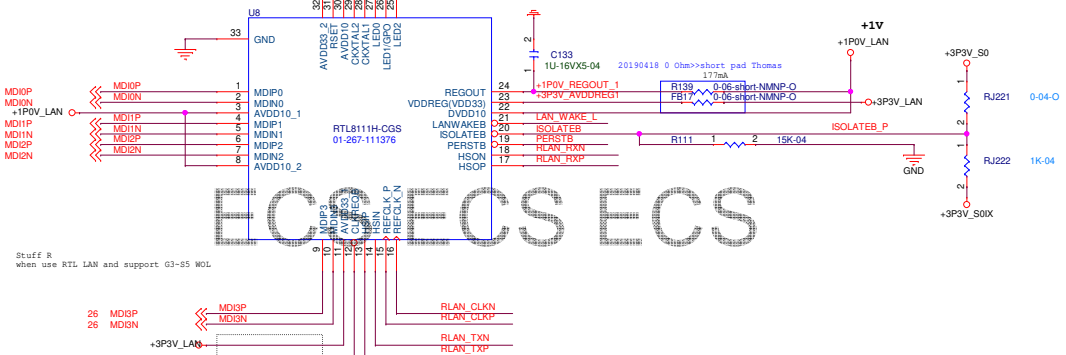
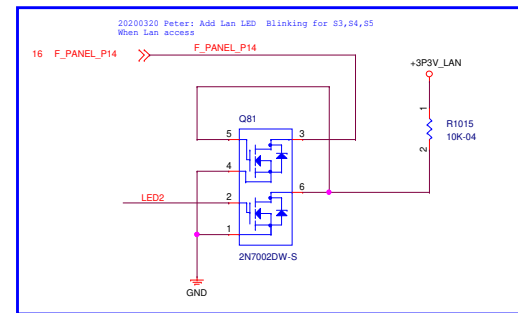
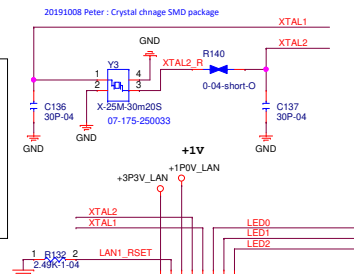
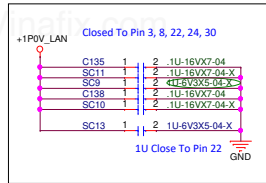
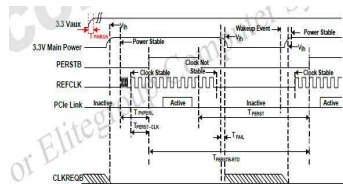
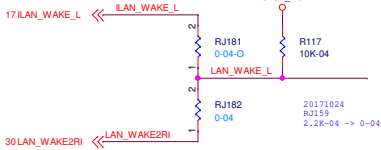
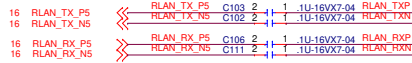
B460				H410			
RJ141	RJ142	RJ143	RJ144	RJ145	RJ146	RJ147	RJ148
RJ149	RJ150	RJ151	RJ152	RJ153	RJ154	RJ155	RJ156
RJ157	RJ158	RJ159	RJ160	RJ161	RJ162	RJ163	RJ164
RJ165	RJ166	RJ167		RJ172	RJ169	RJ170	RJ171



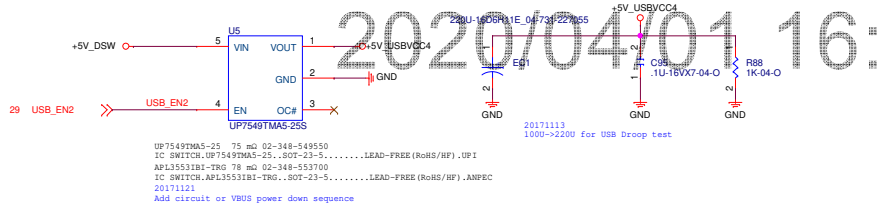
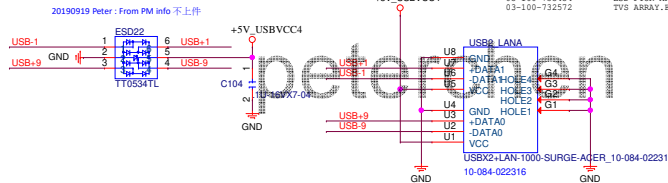
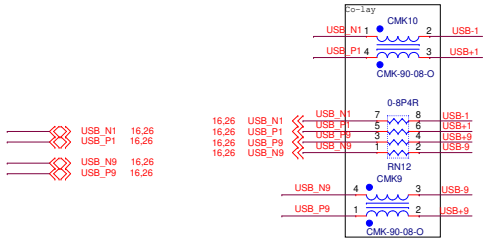
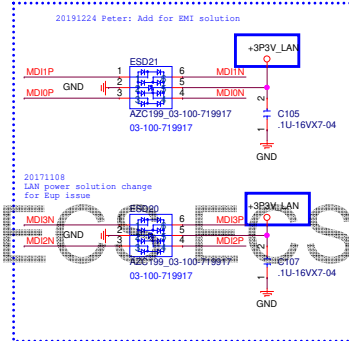
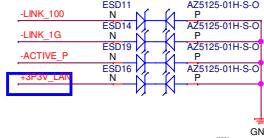
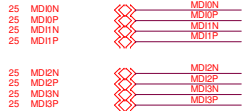
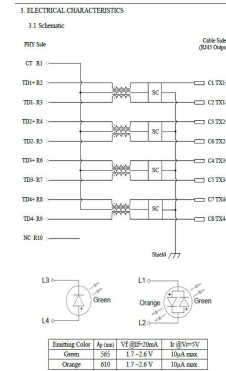
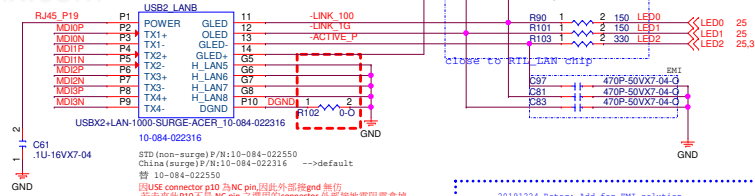
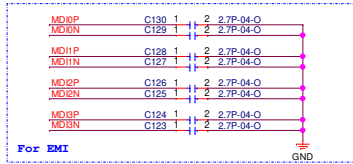
# LAN RTL8111H

## 20190909 Peter: Reference Coric project Lan circuit

20180105 V1.0  
1U-16VX7-04->1U-6V3X7-04  
For LAN DC Noise.



## USB2.0+LAN



		S0		S3	S4	S5	G3 to S6
<div>Rear Side</div> <div><div>Active</div><div>Speed</div></div>	Active LED (Single Color)	Access	Blink	Blink	Blink	Blink	
		Not Access	OFF	OFF	OFF	OFF	
	Speed-LED (Dual Color)	Disconnected	OFF	OFF	OFF	OFF	
		100% ON with Amber Color	ON				
		100% ON with Green Color	ON				
	10% OFF	OFF					

Front USB3.0 Type C


Vinafix.com

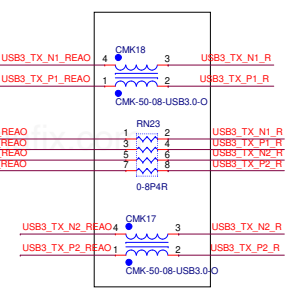
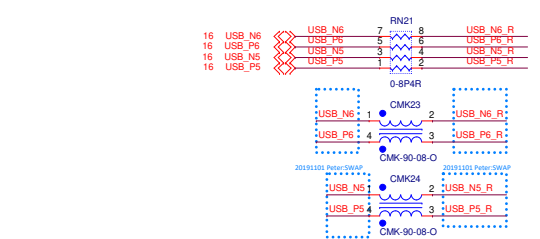
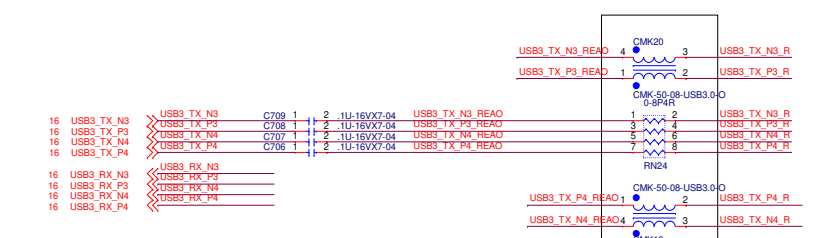
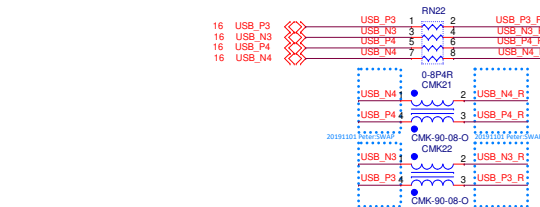
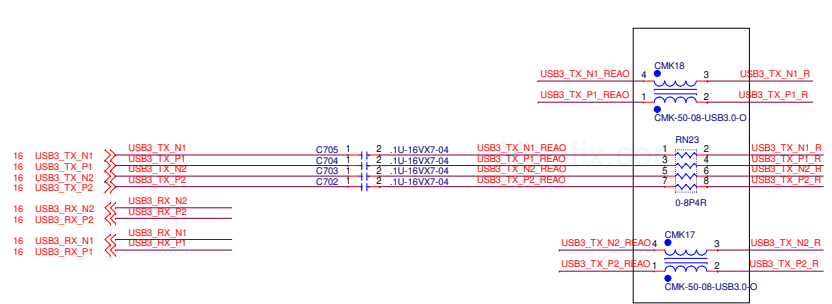
20190909 Peter: Tianyan not support Type C

ECS ECS ECS

peterchen

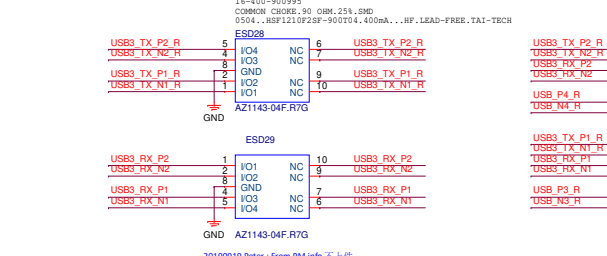
2020/04/01 16:19

				Elitegroup Computer Systems			
Reserve(U3 Type C)							
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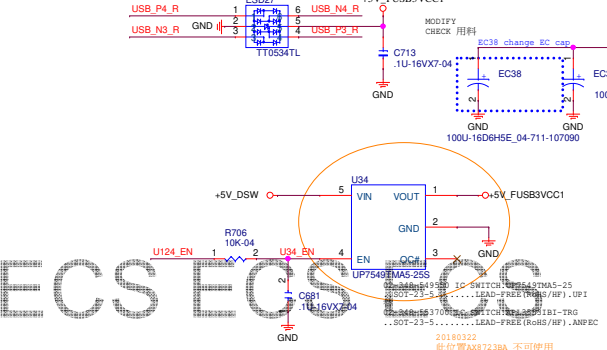


20190418 change 0歐到 100Ω Thomas

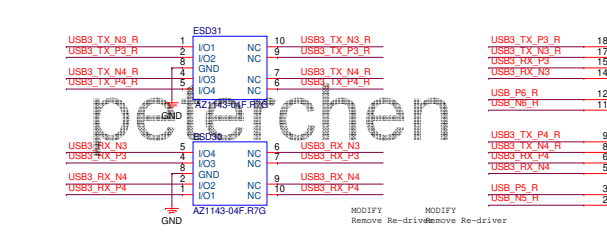
20190418 change 0歐到 100Ω Thomas



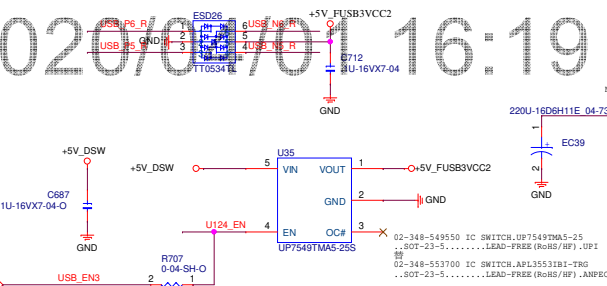
20190919 Peter : From PM info 不上件



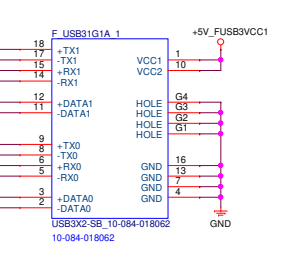
20180322 此位置A487238A 不可使用 Drop test fail



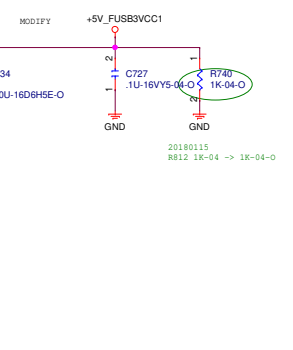
20190919 Peter : From PM info 不上件



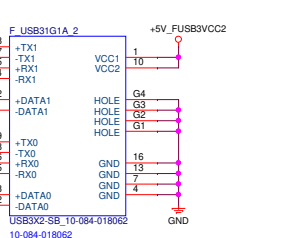
20190919 Peter : From PM info 不上件



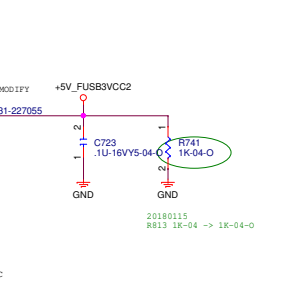
20180115 R812 1K-04 -> 1K-04-0



20180322 此位置A487238A 不可使用 Drop test fail



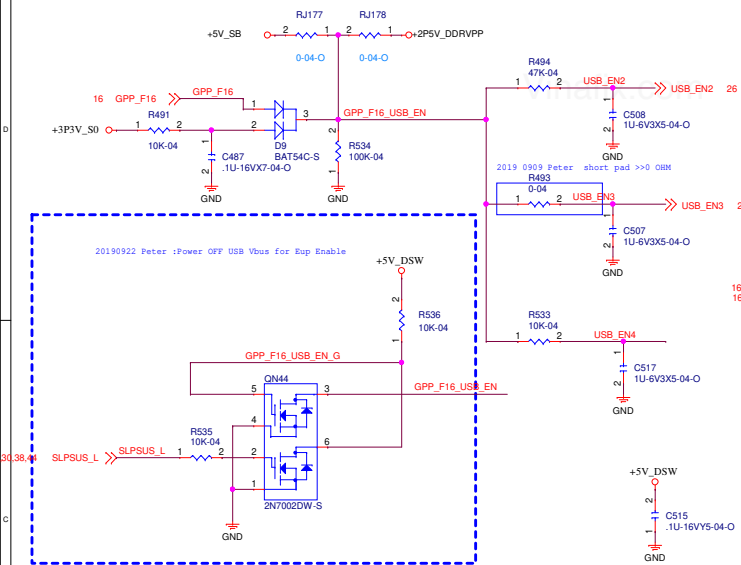
20180115 R813 1K-04 -> 1K-04-0



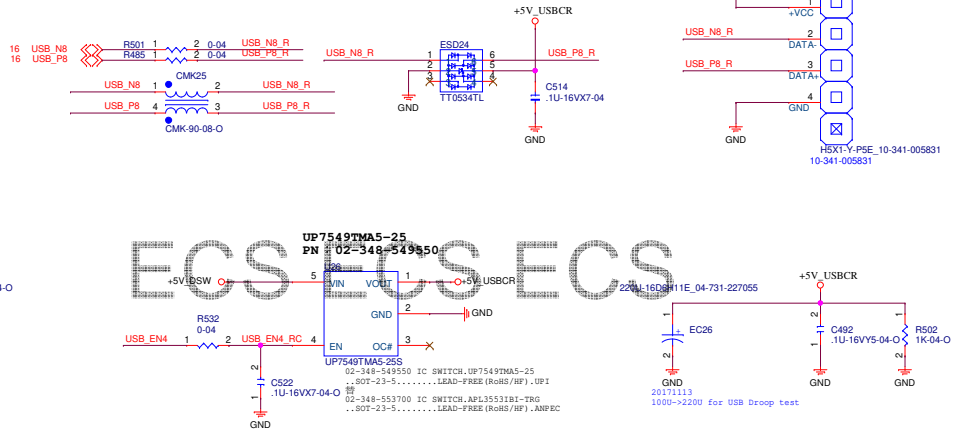
20190919 Peter : From PM info 不上件

	power switch Enable use	RJ5	D26	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (2-3)	NA	0 Volt	Acer S4 W S5 W/O USB_5VDUAL
	5VSB	0ohm (1-2)	NA	5 Volt	
*	GPIO	NA	Stuff	S4 : 5 Volt S5 : 0 Volt	

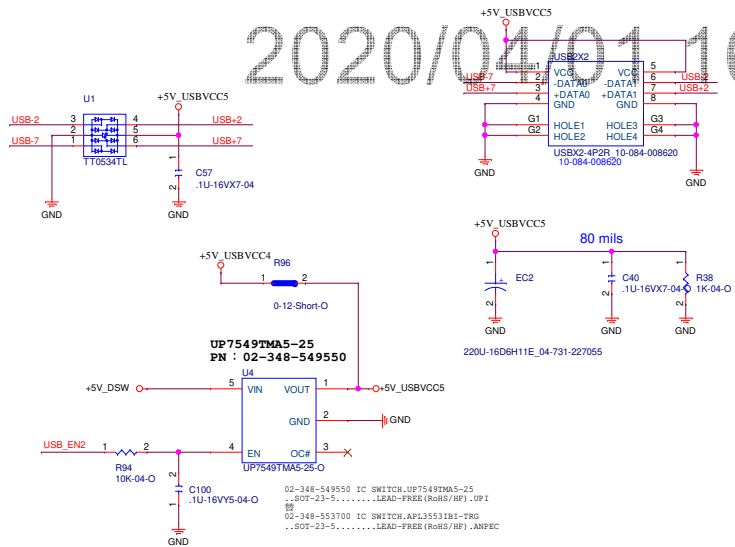
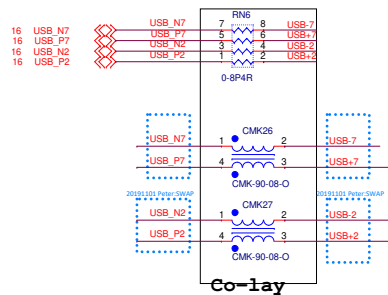
STATUS	S0	S3	S4	S5
GPP_F16	HI	HI	HI	LOW
USB_PWR	ON	ON	ON	OFF



## Card Reader



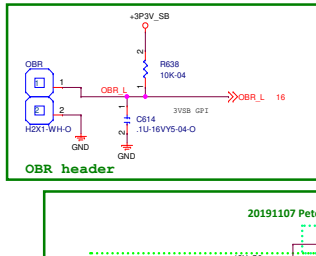
## Rear USB2.0



Title			
CR header&Dual USB2.0			
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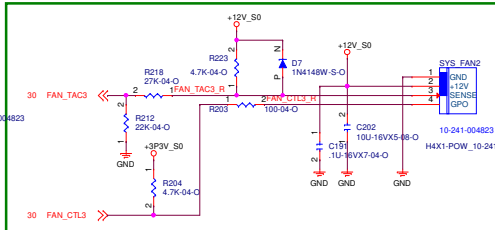




## CPU\_FAN 4 pin circuit

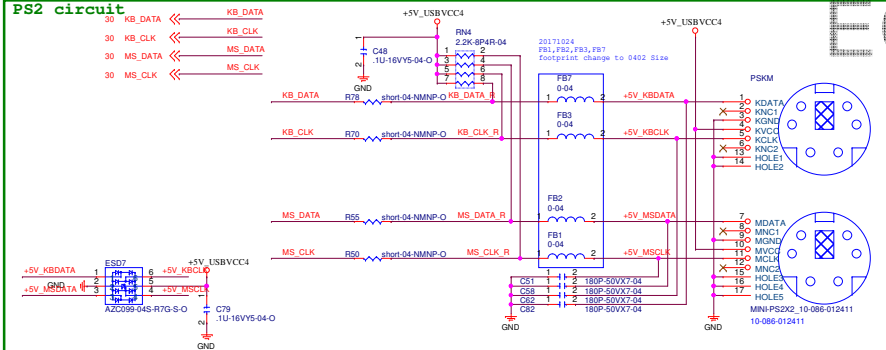
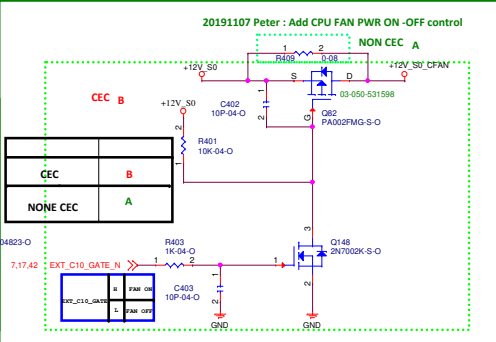
## Buzzer circuit

OBR header

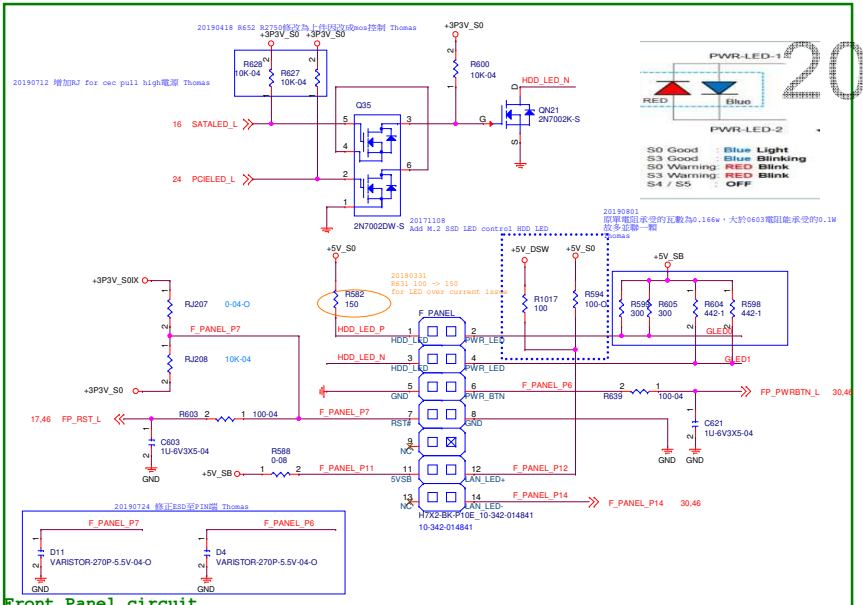
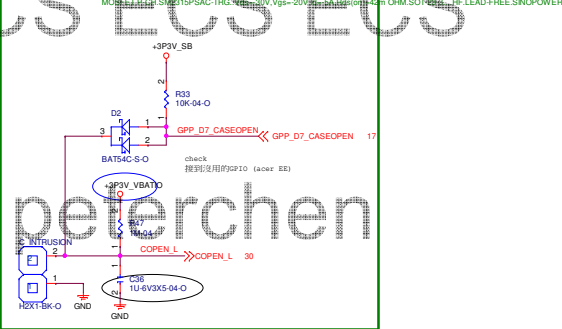


### SYS\_FAN 4 pin circuit

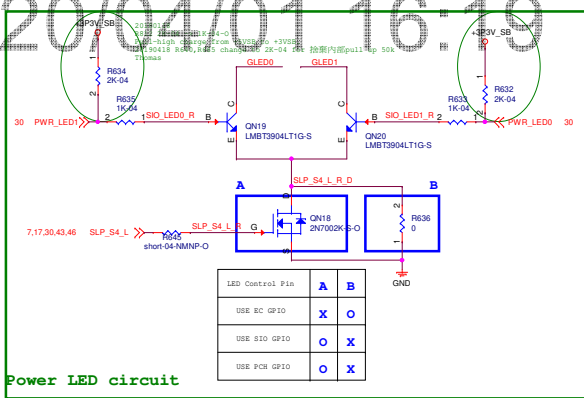
### SYS\_FAN 4 pin circuit



## Case open circuit



## Front Panel circuit



## Power LED circuit

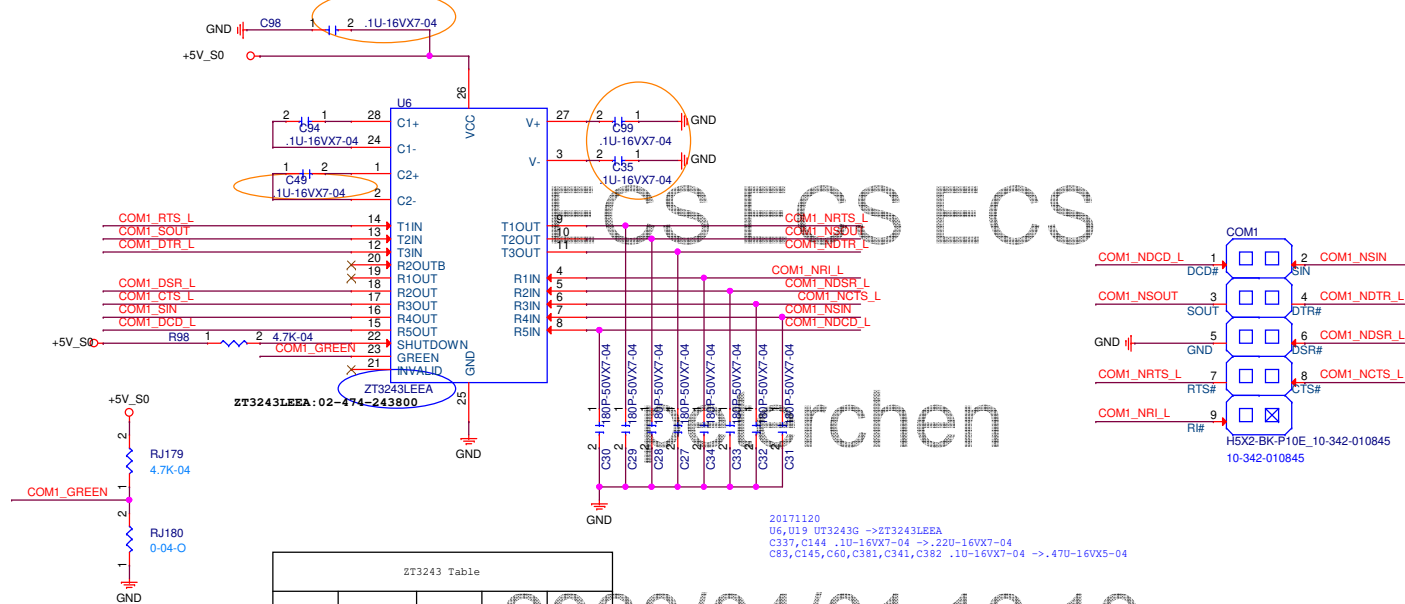
Note:  
Reserve for Delay 4S關機時，由於BIOS並不知道這個指令，  
所以Delay 4S後並無法改變LED的狀態，若以PCN GPIO  
or Super I/O控制LED狀態，可能會造成Delay 4S後LED會呈  
現無法預期的狀態，所以使用SLP\_S4#在Delay 4S下電後將LED燈的訊號段開。

## LPT Header

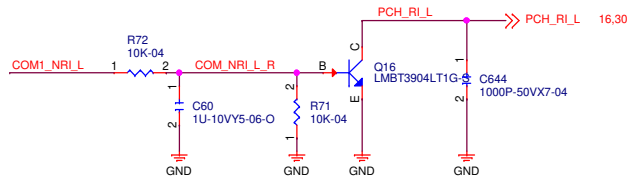
20190909 Peter: Tianyan not support LPT

## COM port (header)

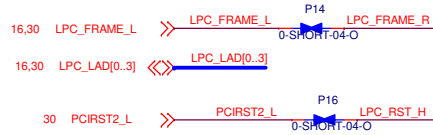
30 COM1\_SOUT >> COM1\_SOUT  
30 COM1\_RTS\_L >> COM1\_RTS\_L  
30 COM1\_DTR\_L >> COM1\_DTR\_L  
30 COM1\_DCD\_L >> COM1\_DCD\_L  
30 COM1\_SIN >> COM1\_SIN  
30 COM1\_DSR\_L >> COM1\_DSR\_L  
30 COM1\_CTS\_L >> COM1\_CTS\_L



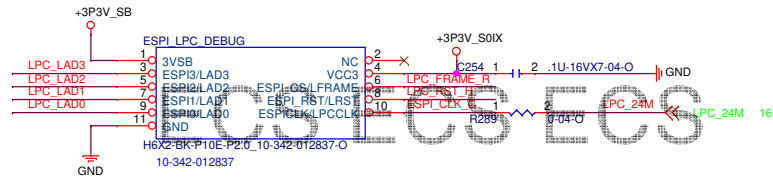
ZT3243 Table				
GREEN	SHUTDOWN	TxOUT	RxOUT	RxOUT_P
0	0	Z	Active	Active
0	1	Active	Active	Active
1	0	Active	Active	Active
1	1	Z	Z	Active



Vinafix.com



若Debug card用的IC是Fintek的料則IC會自己判斷LPC/eSPI  
若用的是ITE則卡上會有多一組轉電電路



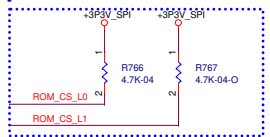
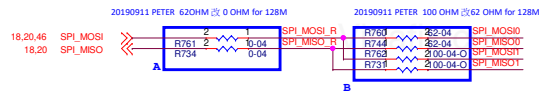
PN:10-342-012837  
HEADER...6\*2 180D..P2mm.....6T.PIN 12 EMPTY...BLACK.111121524C....LEAD-FREE.L4S

peterchen

2020/04/01 16:19

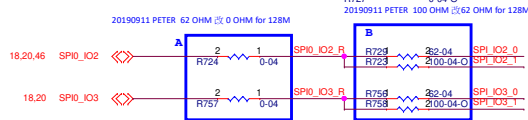
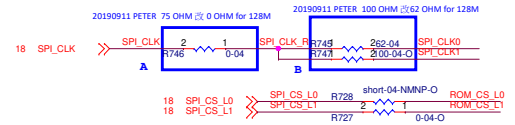
## TPM circuit

## 20190910 Peter:Tianyan not support TPM

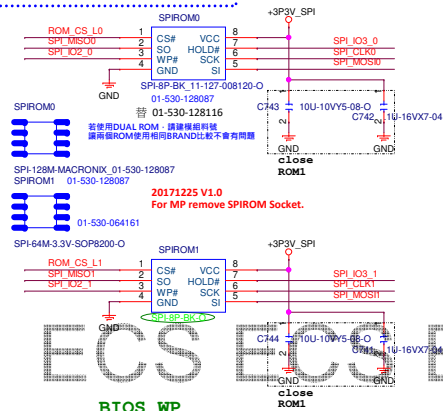
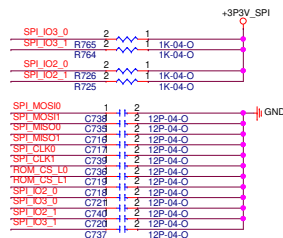


## SPI ROM

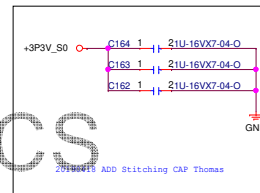
```
20171205 V1.0
Add R928-R932 4.99-02 for PDG1.5 update.
20171205 V1.0
R556,R568,R560,R577,R561,R554,R549,R548,R578,R569 Size change 0201
```



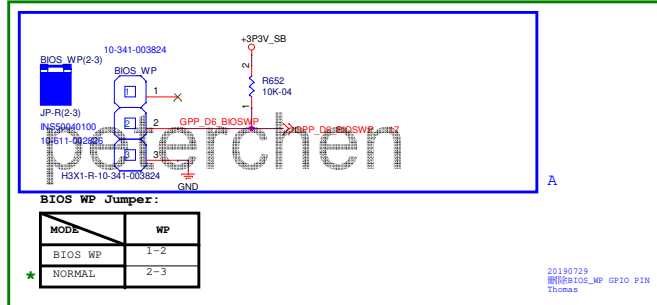
	A	B
Single Load	0 ohm	62 ohm
Dual Load	75 ohm	100 ohm



A3 stuff BAT54C for debug and reserve 0 ohm  
A4 0 ohm change to SH

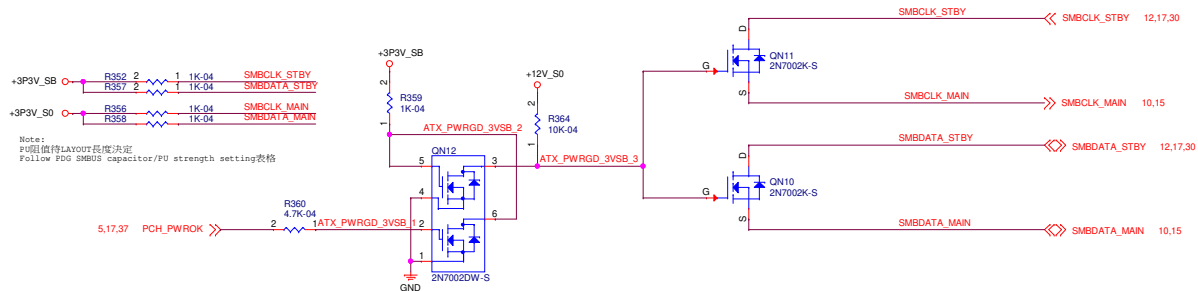


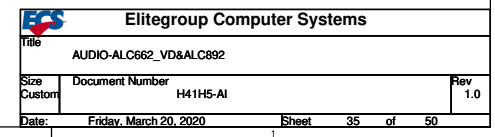
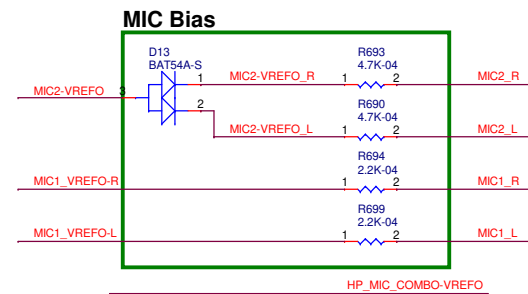
## BIOS WP



20190729  
删除BIOS\_WP GPIO PIN  
Thomas

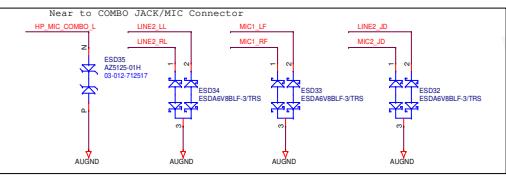
## SMbus Logic Circuit



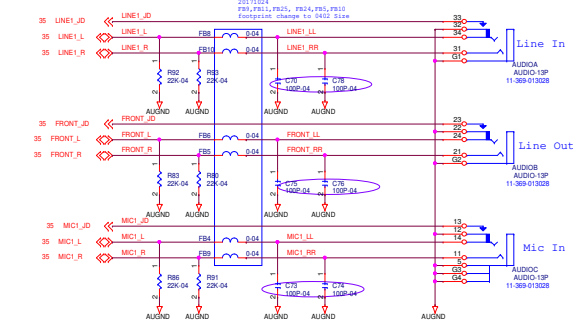


Combo jack

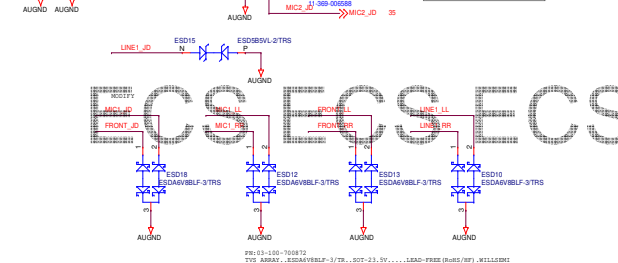
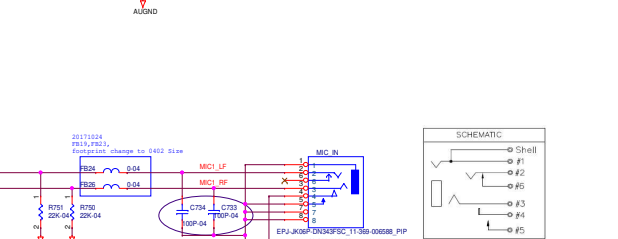
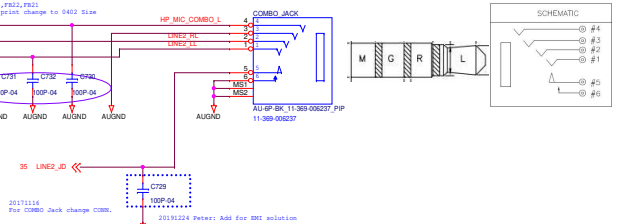
- 35 MIC2\_L
- 35 MIC2\_R
- 35 LINE2\_R
- 35 LINE2\_L



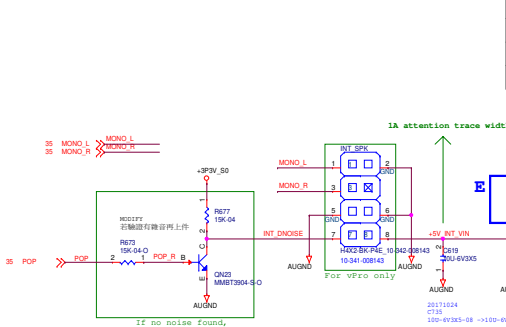
Rear IO 3 in 1



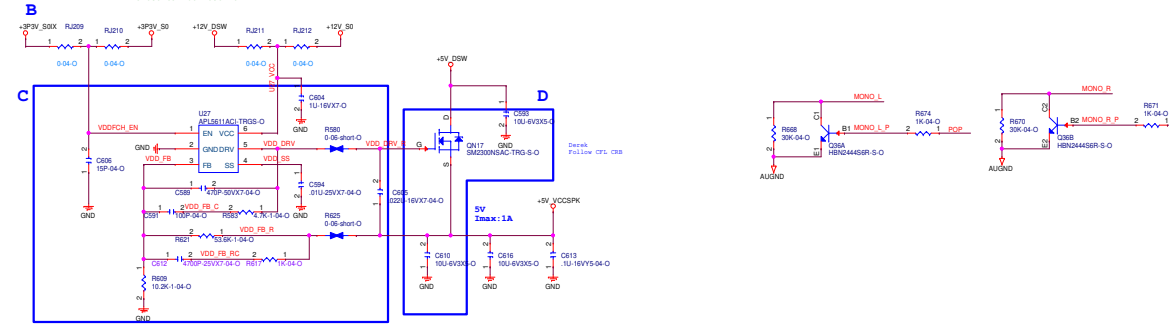
A	S	C
LINE IN	LINE IN-JD	LINE IN-L
LINE IN	LINE IN-JD	LINE IN-R
LINE OUT	LINE OUT-JD	LINE OUT-L
LINE OUT	LINE OUT-JD	LINE OUT-R
MIC IN	MIC IN-JD	MIC IN-L
MIC IN	MIC IN-JD	MIC IN-R



Internal speaker



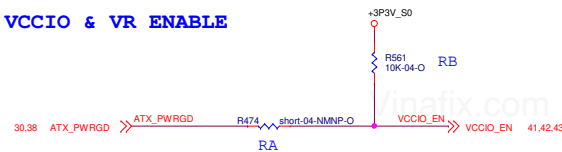
APL5611 上件?	Modern standby	A	B	C	D	E	F
上件	供电	X	V(2-3)	V	V	V	X
上件	不供电	X	V(1-2)	V	V	V	X
不上件	供电	V	X	X	V	V	X
不上件	不供电	X	X	X	X	X	V



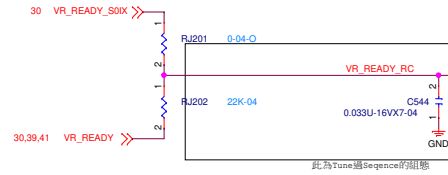


# PCH\_PWROK & VCCST

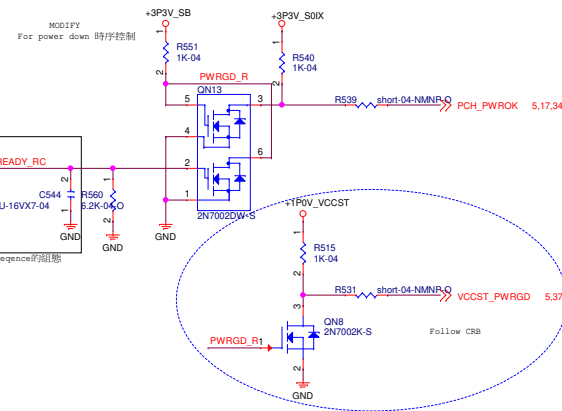
## VCCIO & VR ENABLE



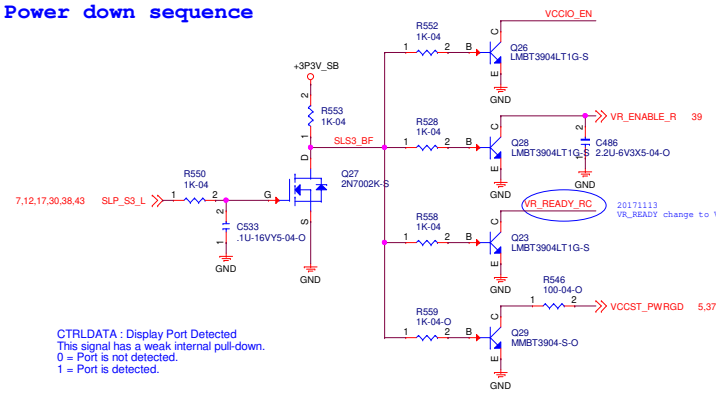
	RA	RB
ATX_PWRGD	V	X
VCC3	X	V



## RSMRST#



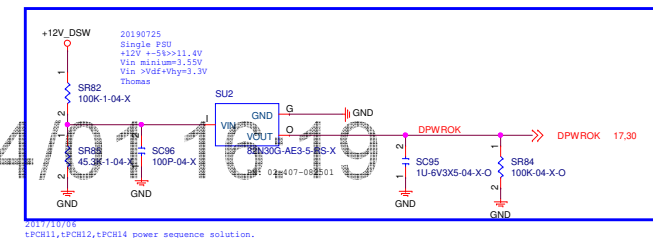
## Power down sequence



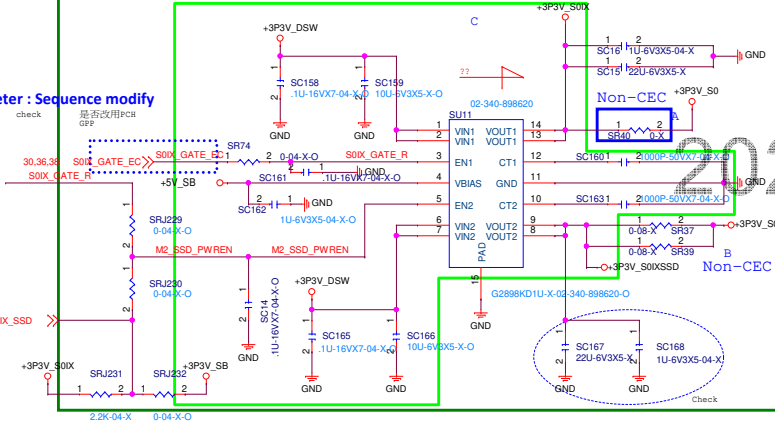
CTRLDATA : Display Port Detected  
This signal has a weak internal pull-down.  
0 = Port is not detected.  
1 = Port is detected.

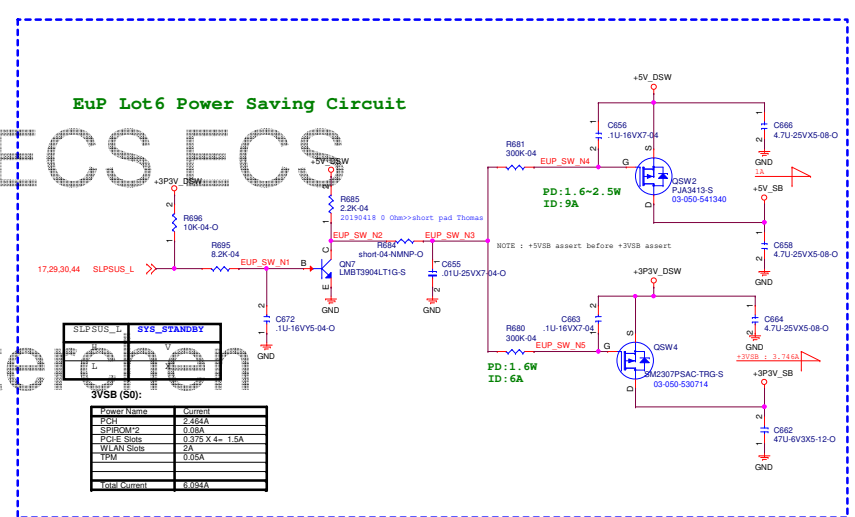
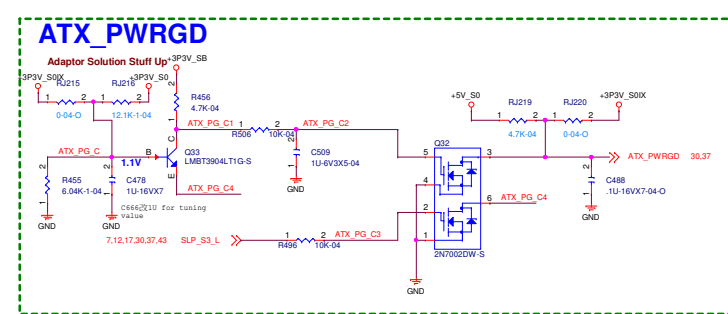
	A	B	C
CEC	X	X	V
Non-CEC	V	V	X

## DPWROK



## 2019 1107 Peter : Sequence modify



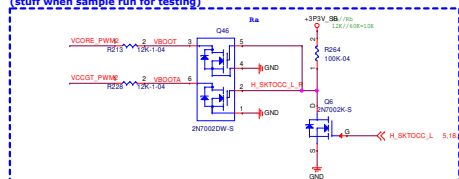
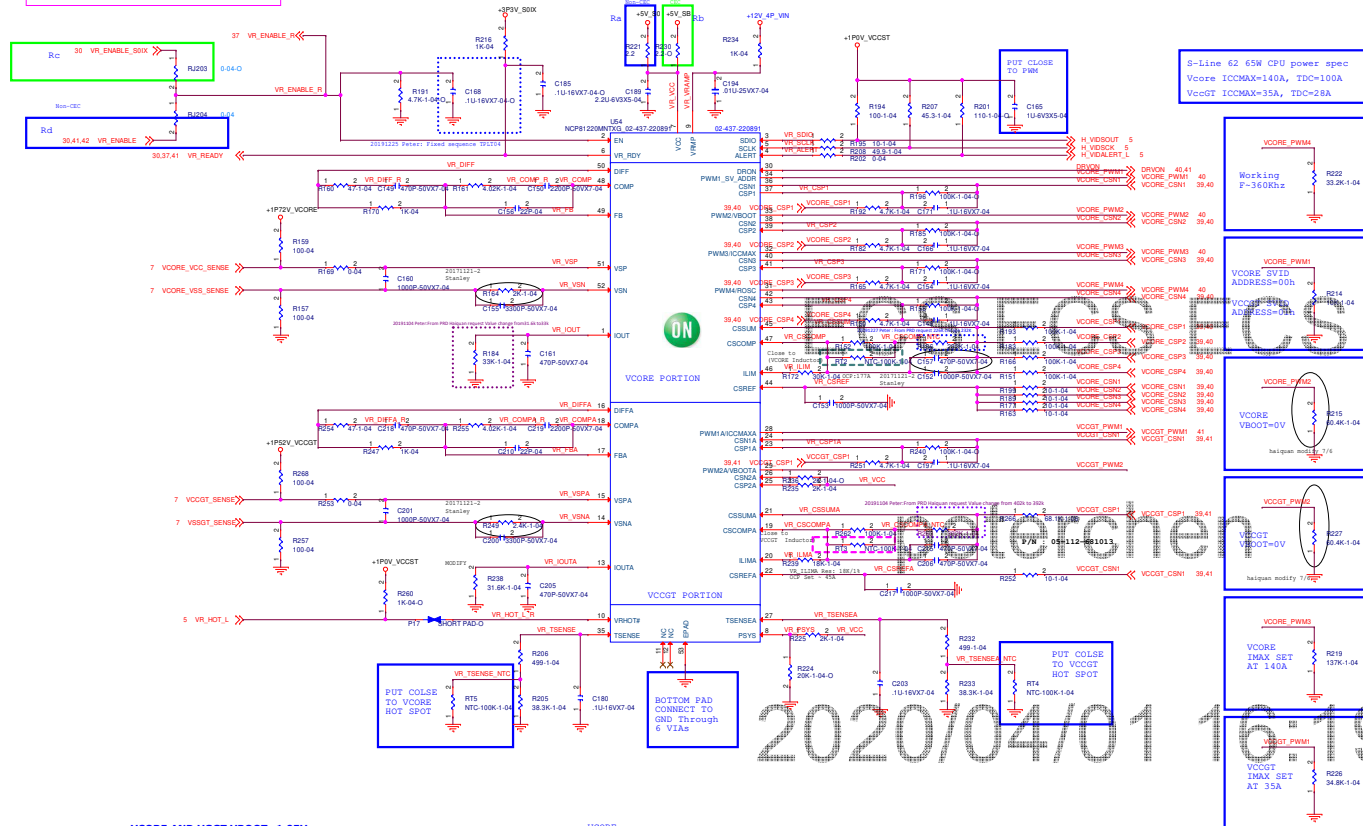


PSU 12V2 Capability Recommendations		
Processor TDP	Continuous Current	Peak Current
165W	37.5A	45.0A
125W	26A	34A
65W	23A	30A
35W	13A	16.5A

- 12-16A support for 2x2 (4pin) connector
- 18-24A support for 2x3 (6pin) connector
- 24-32A support for 2x4 (8pin) connector

This recommendation is based on common design practice. PSU and system designer may design or use differently and should be responsible for designing the PSU to meet all electrical, thermal, safety and reliability requirements based on the application of the PSU.

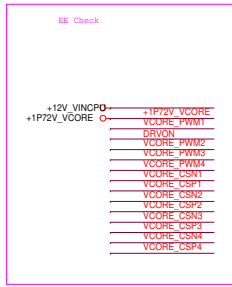
	Ra	Rb	Rc	Rd
CEC	X	V	V	X
Non-CEC	V	X	X	V



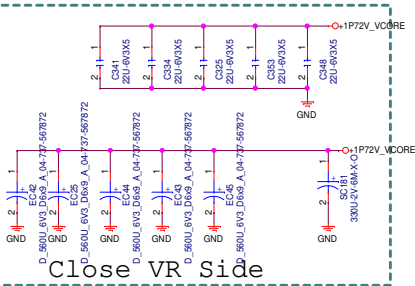
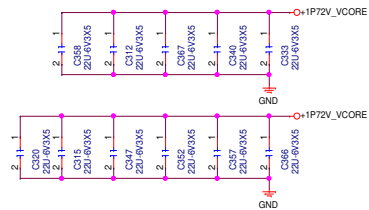
VBOOT	Ra	Rb (R73, R74)
A3-A4	Stuff	60.4K-1-04

# POWER UPDATE20190912

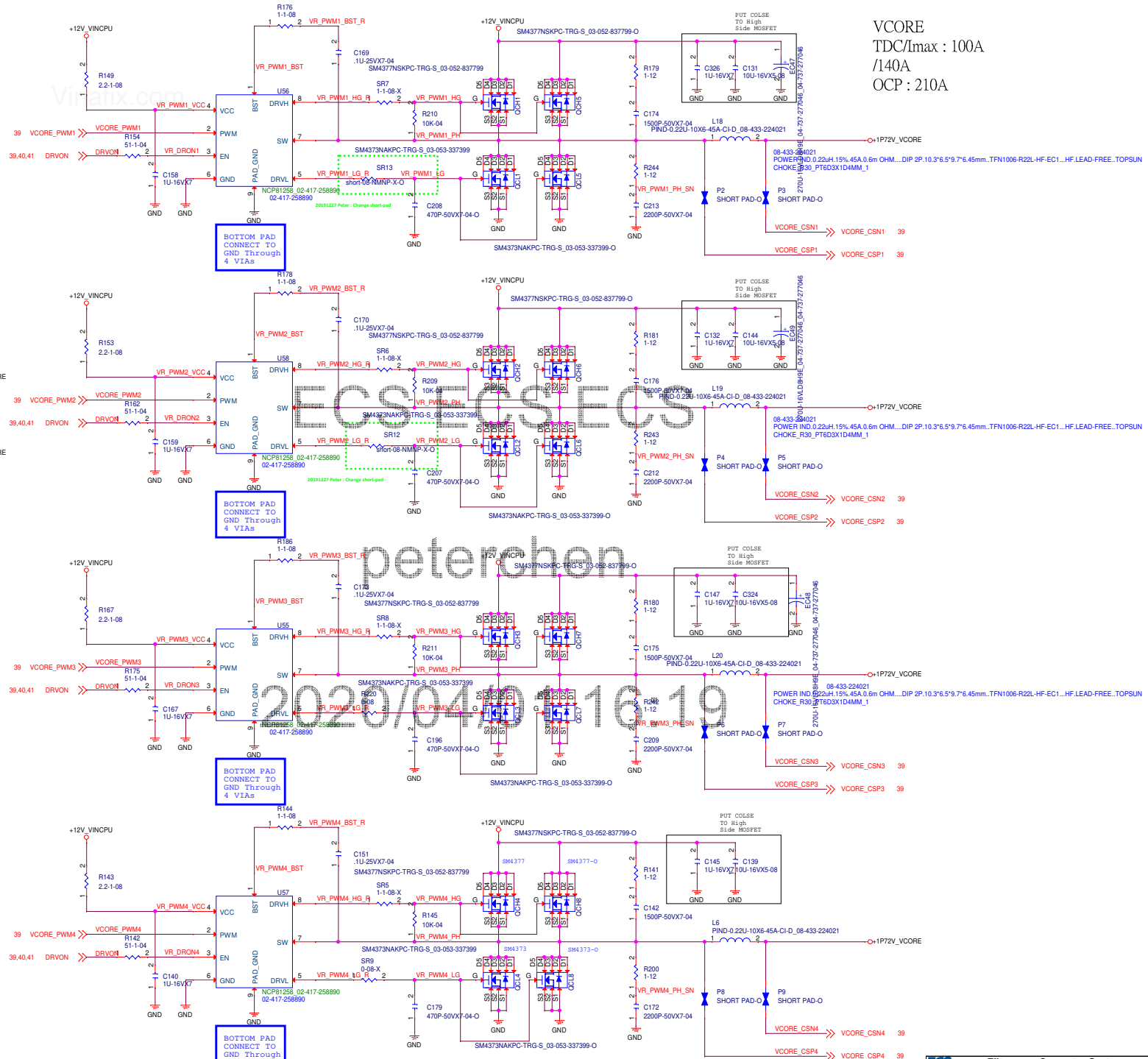
VCORE  
TDC/Imax : 100A  
/140A  
OCP : 210A

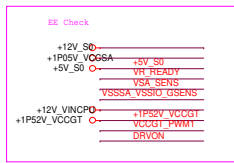


VCORE MLCC Quantity  
CPU Inside 22U\*34  
EC 560U\*5

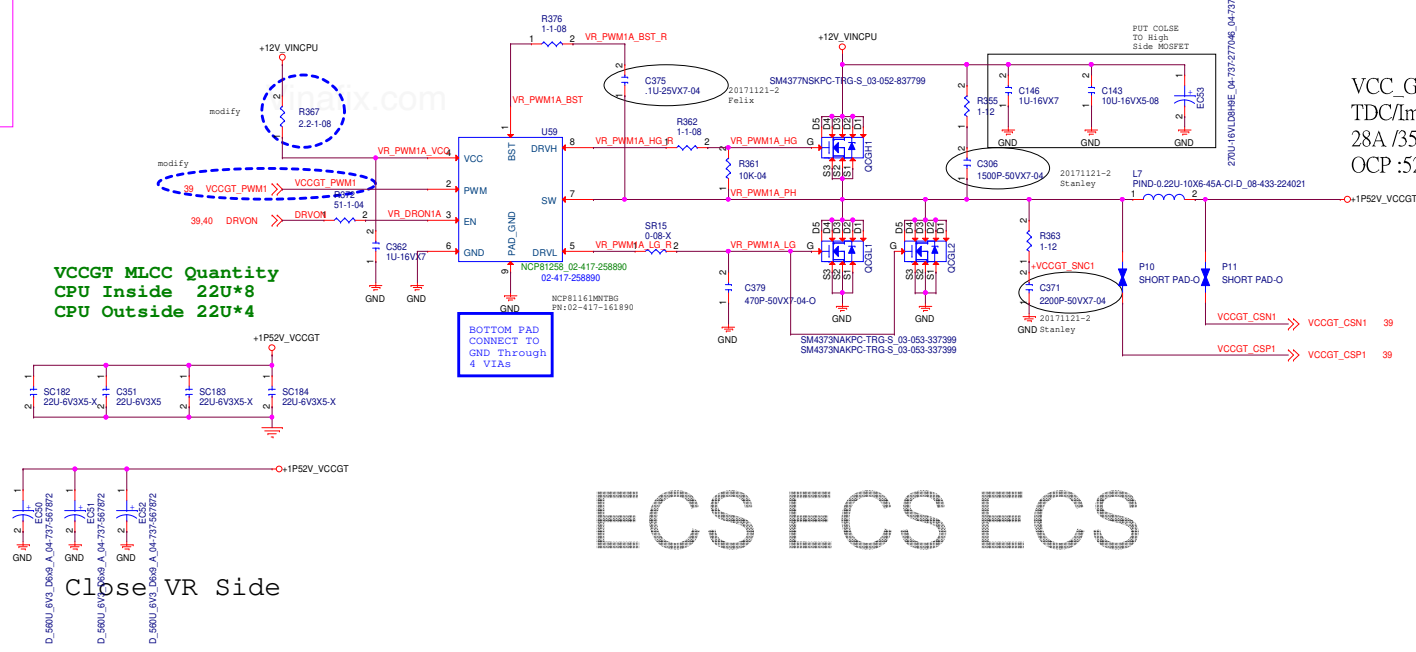


Close VR Side



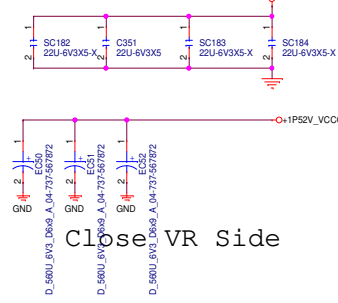


POWER UPDATE 20191007



VCC\_GT:  
TDC/Imax :  
28A /35A  
OCP :52.50A

VCCGT MLCC Quantity  
CPU Inside 22U\*8  
CPU Outside 22U\*4

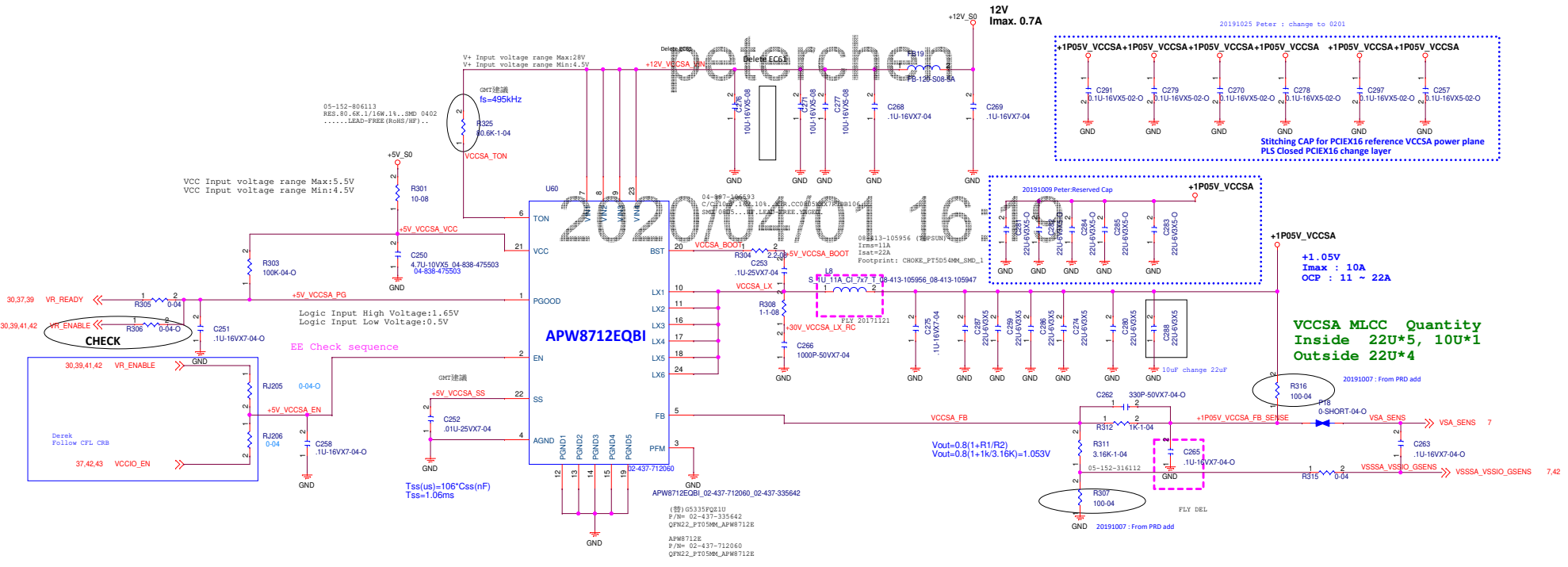


Close VR Side

ECS ECS ECS

2020/04/01 16:19

peterchen



+VCCIO

POWER UPDATE 20191007

VCCSA MLCC Quantity  
Inside 22U\*6  
Outside 22U\*4

12V  
I<sub>max</sub> 0.34A

EE Check

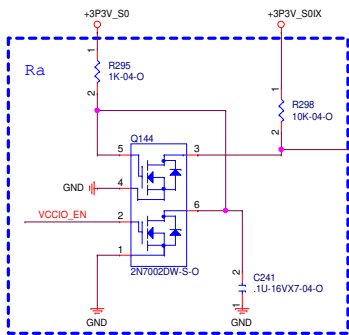
+0P95V\_VCCIO  
+12V\_S0  
+3P3V\_SB  
+3P3V\_S0IX  
+5V\_S0  
VCCIO\_SENSE  
ATX\_PSON\_ID\_L

05-152-806113  
RES: 80.6K, 1/16W, 1% SMD 0402  
..... LEAD-FREE (RoHS/RF) .....

VCC Input voltage range Max: 5.5V  
VCC Input voltage range Min: 4.5V

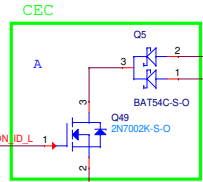
EE Check sequence

Logic Input High Voltage: 1.65V  
Logic Input Low Voltage: 0.5V



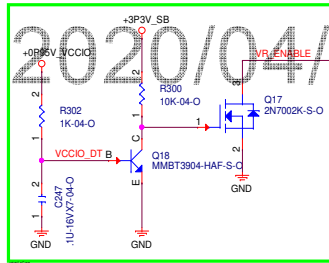
	Ra	Rb
VCCIO有爬升要求	v	x
VCCIO无爬升要求	x	v

\*Ra上件，建議Ra要上件，避免偷打



	A
CEC	V
Non-CEC	X

Reserve for CEC



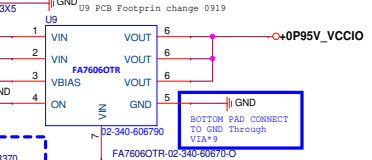
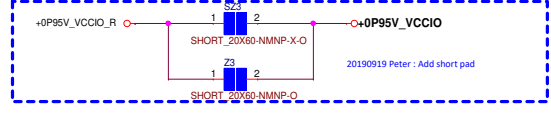
預留for Sequence debug  
hardware 通501X VR\_S0 keep high

+VCCIO/0.95V  
I<sub>max</sub> : 6.4A  
OCP : 8.32~22A

V<sub>out</sub>=0.8\*(1+R1/R2)  
V<sub>out</sub>=0.8\*(1+1K/5.23K)=0.953V

	R180	U9	R187	R188	PFM
APW8712	1-2	V	V	X	H Force PWM Mode L Automatic PWM mode
APW8742	1-2	V	V	X	H Force PWM Mode L Automatic PWM mode
APW8745	2-3	X	V	V	H Normal Mode L Low power mode

\* Default

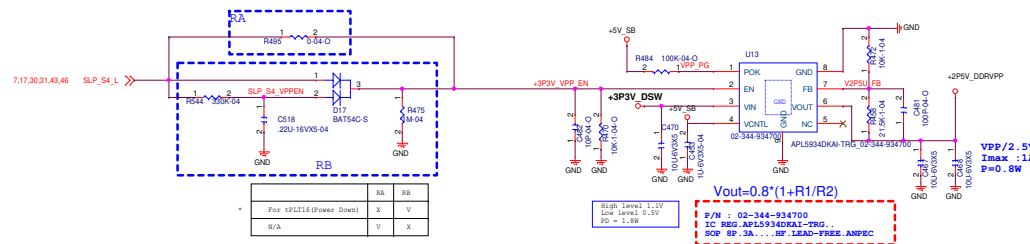
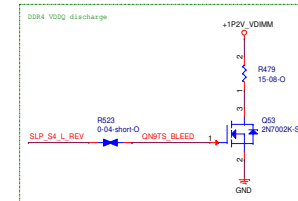
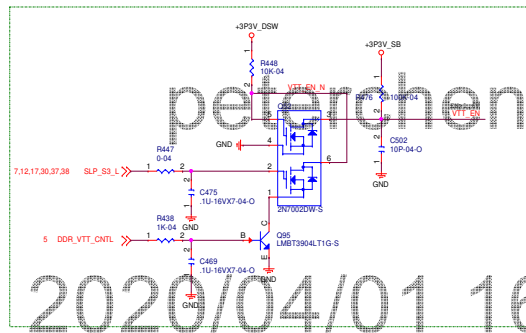
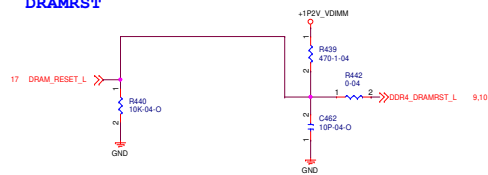
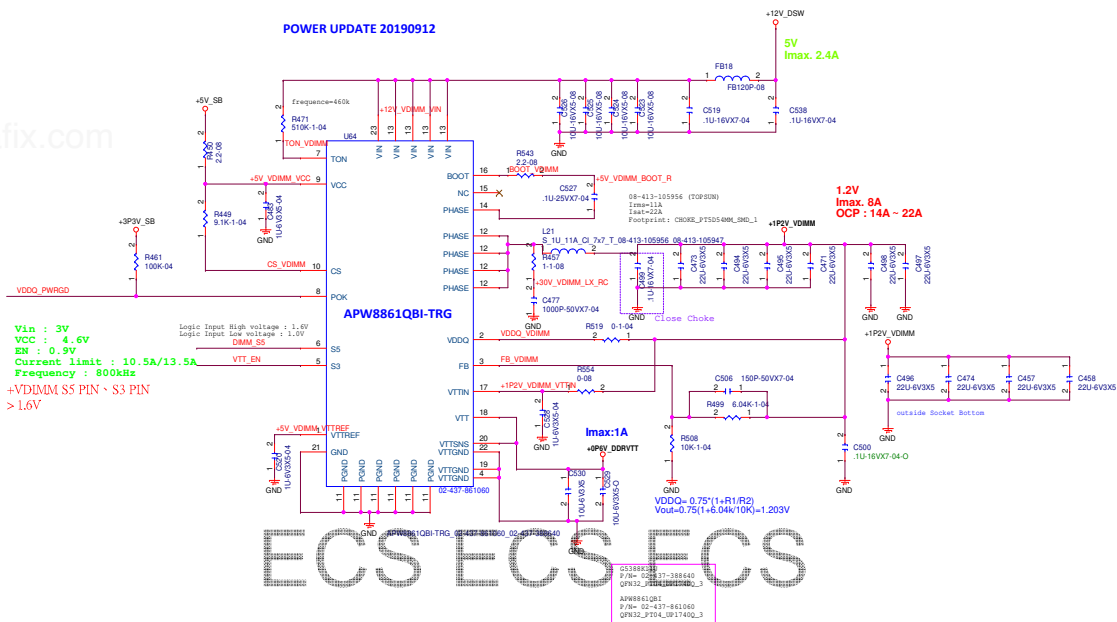
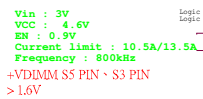
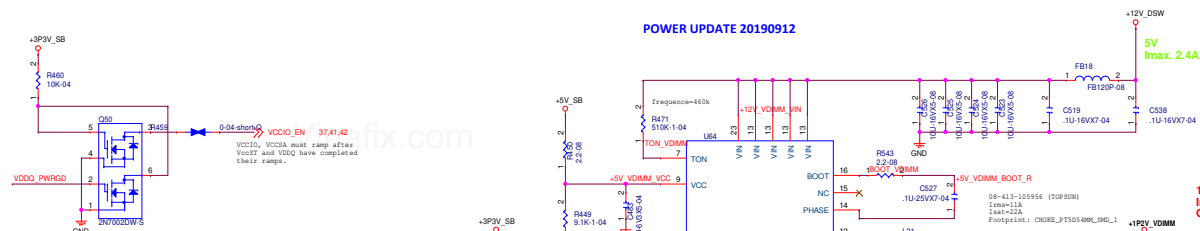


PWM IC	U9	Rc	Rd	Rf	Rg	Z3	SZ3
APW8712	V	V	X	V	X	CUT	CUT
APW8742	V	V	X	V	X	CUT	CUT
APW8745	X	V	V	X	X	X	X

PWM IC	U9	Rc	Rd	Rf	Rg	Z3	SZ3
APW8712	V	X	V	X	V	CUT	CUT
APW8742	V	X	V	X	V	CUT	CUT
APW8745	X	V	V	X	X	X	X

Elitegroup Computer Systems			
File	DC/DC VCCIO		
Size	Document Number	H41H5-AI	Rev 1.0
Date:	Friday, March 20, 2020	Sheet 42 of 50	





	RA	RB
For tPLT16 (Power Down)	X	V
N/A	V	X

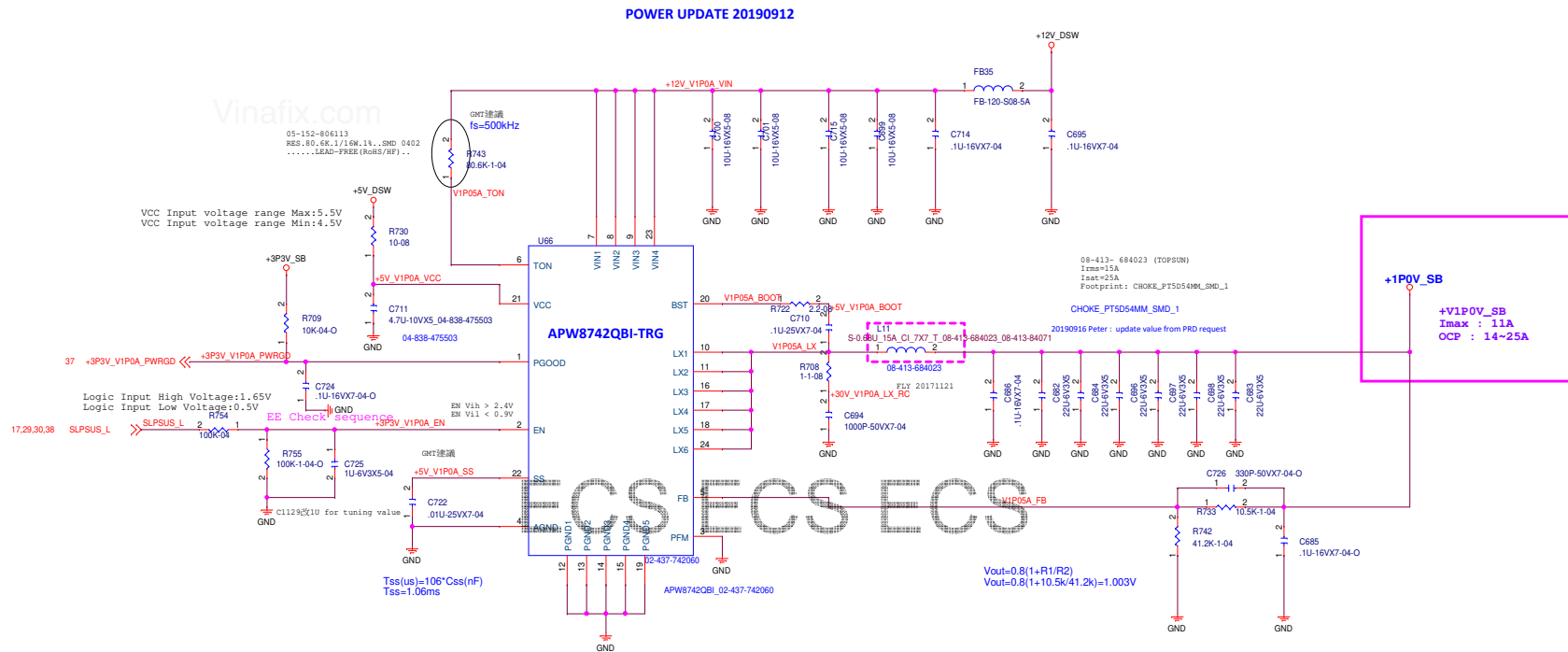
VDDQ/VPE timing requirements:						
Label	Required by	Controlled by	Minimum	Maximum	Units	Note #
1PLT16	PLT (MEM)	PLT	30		ms	30
1PLT20	PLT (MEM)	PLT	2.5		ms	30



+V1P0A(1.0V)

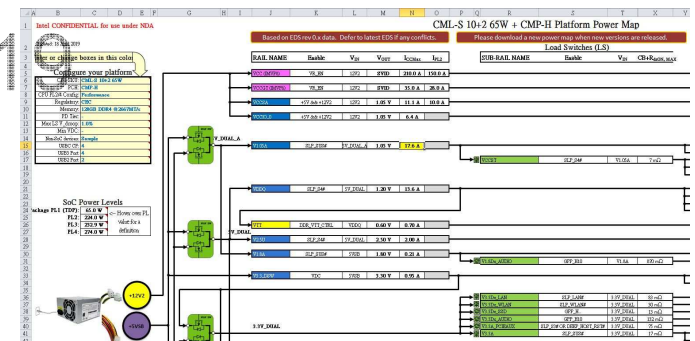
EE Check

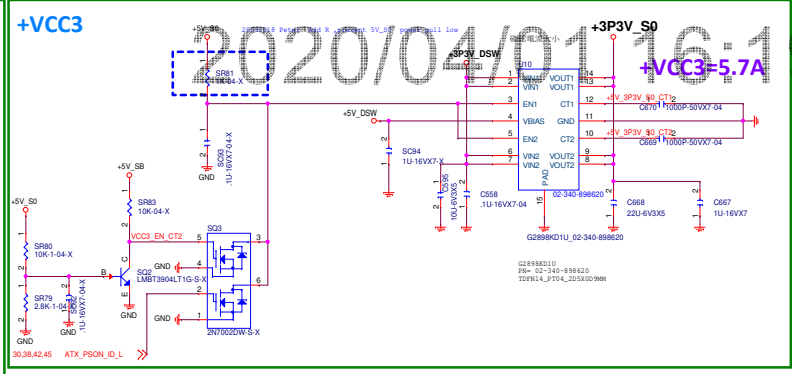
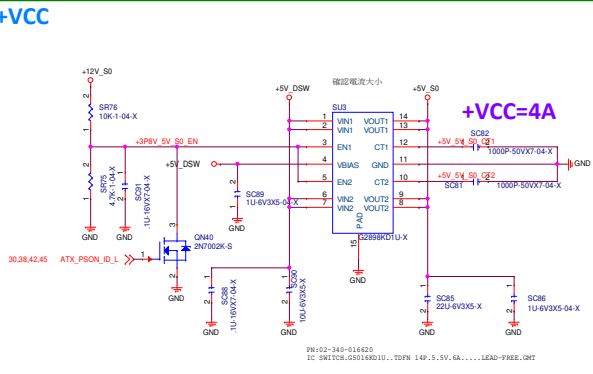
+12V\_DSW  
+3P3V\_SB  
+5V\_DSW  
+1P0V\_SB  
+3P3V\_V1P0A\_PWRGD  
+12V\_S0



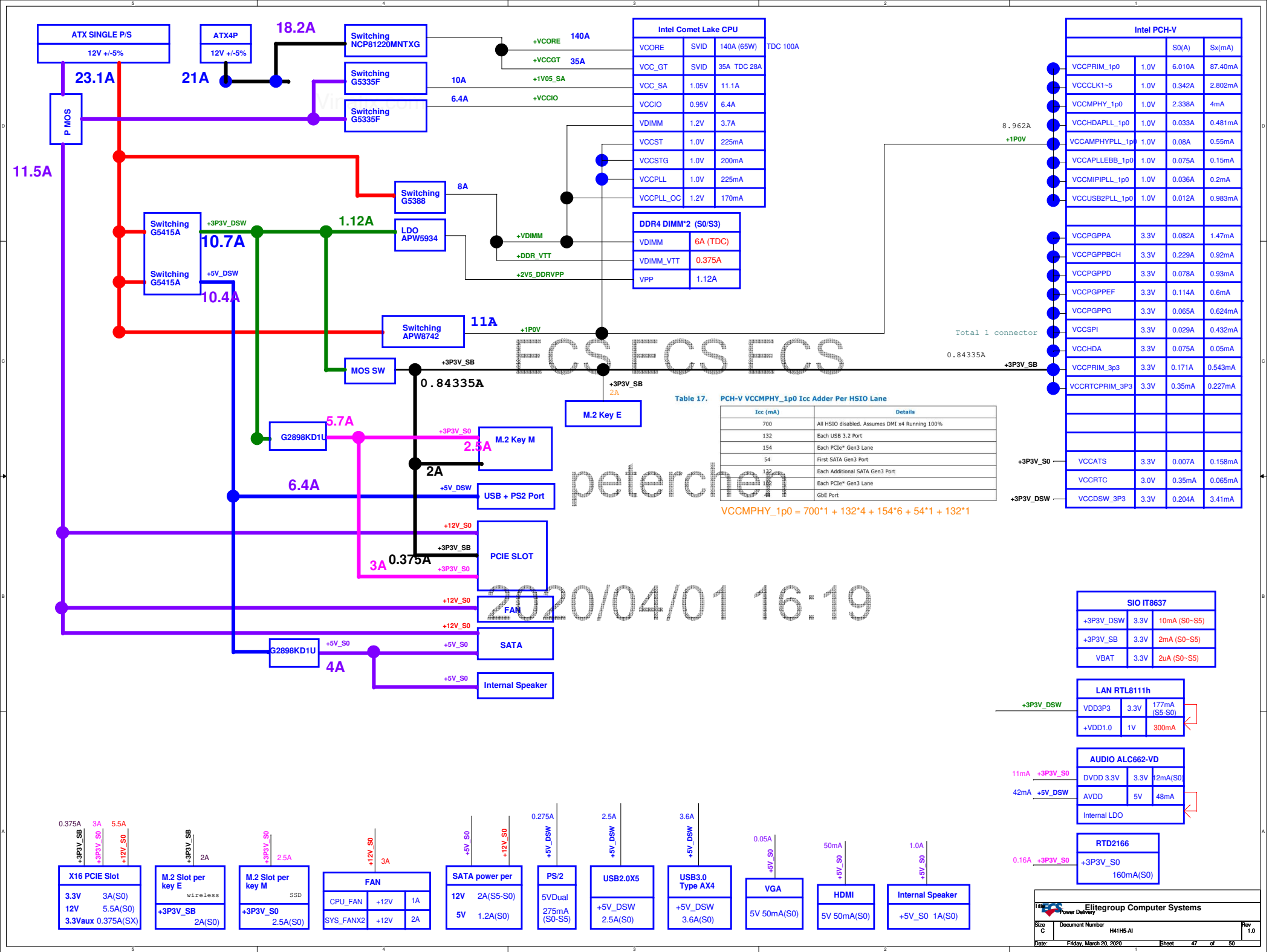
參考Comet Lake Platform Controller Hub  
External Design Specification (EDS) – Volume 1 of 2  
December 2018 Revision 0.7 Document Number: 606576  
需要確認Comet Lake S-line PCH電壓

2020/04/01 16:10









# History

Rev	Date	Notes	Rev	Date	Notes
B	20171113	R250 0-04 ->33-04;Add 0.033U-16VX7-04 for PROCPWRGD surge.	20171205		Add U41 APL5611ACI for Internal speaker issue.
	20171024	Add VDDQ_PWROK control VCCST PWR circuit for Intel VCCPLL_OC leakage issue	20180808		1U-16VX5-04 ->1U-6V3X5-04 for MLCC 缺料
	20171024	Add C525,C511,C565,C556 10U-6VX5 for SI DC noise test.			
	20171108	R56 3.32K-1-04 -> 3.48K-1-04 ; CG:1101->001 for HDIM SI test.			
	20171106	Add CMK4 16-400-900143 for DP SI test.			
	20171123	Del R623 0-04 ;Add R30,R37 0-04;Add SUSWARN control VBUS circuit. R716 0-04->10K-04; C767 Add 0.01U-25VX7-04 for VBUS power down sequence			
	20171024	R564 change to stuff 10K-04 for RI WAKE issue			
	20171108	C627,C626 15-04 ->12P-02 for SI 24 XTAL test			
	20171108	C770,C780 12-04 ->15P-02 for SI 32.768 XTAL test			
	20171108	SR39 Add 100K-04-X(1-2);R624 Add 20K-04 Del R624; R704 4.7K-04-X(1-2)->100K-04-X(1-2) SR37,SR40 20K-04-X(1-2) -> 100K-04-X(1-2) R655 1K-04 ->100K-04 follow EDS recommend.			
	20171026	PCIE1X_1 net change form PEX1_RST_L to PEX4_RST_L			
	20171127	Add CNVi CLKREQ&RESET level shifter circuit for Intel MOW update.			
	20171108	LAN power solution change for Eup issue			
	20171113	EC1,EC26 100U->220U for USB Droop test.			
	20171108	R751,R779 22K-1-04 ->56K-1-04;R758,R777 3.3K-1-04 ->698-1-04 for Type C power 1.5A change to 0.9A			
	20171120	Add GP31 for ECIO Energy saving.			
	20171108	Add M.2 SSD LED control HDD LED			
	20171120	U6,U19 UT3243G ->ZT3243LEEA C337,C144 .1U-16VX7-04 ->.22U-16VX7-04 C83,C145,C60,C381,C341,C382 .1U-16VX7-04 ->.47U-16VX5-04 for COM port Error issue.			
	20171027	SIO_24M CLK change from CLKOUT_LPC0 to CLKOUT_LPC1 for SI 24M CLK issue.			
	20171113	Q14 pin C net VR_READY change to VR_READY_RC for power down timing.			
	20171106	Add U29 circuit for Power down DPWROK sequence.			
	20171106	R584,R153 200K->300K; R579 ,R126 0->56K for +ATX_12V droop test			
	20171106	C241,C244 470p->680p C839,C840,C841,C842 1000P->1500P C838,C489 1000P-2200P for Power test.			
	20171106	ATX_3VSB &ATX_5VSB solution change RT8130BGQW->G5415 for Eup solution.			
1.0	20171228	Del CMK4;Add CMK4(1-2) 、CMK4(3-4) 0-04 for DP SI solution.			
	20171225	Remove ME_DISABLE header			
	20180115	VBUS power down circuit change to reserve for Intel MOW WW02 update.			
	20171205	Add R920,R921,R922,R923 for CNVi PDG update.			
	20171225	Rmove LPC debug header.			
	20180118	R640,R665 change to reserve for leakage issue.			
	20180115	Modify charge power control circuit for Acer New EE disgn spec.			
	20171205	Add R928~R932 R556,R568,R560,R577,R561,R554,R549,R548,R578,R569 Size change to 0201 for PDG 1.5 Update			
	20171205	SPIROM Socket remove			



